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Manchester Encoder and Decoder with Clock Recovery Unit and Invalid Detector

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Abstract
Communication has become a major part of our day to day life. The idea, knowledge or data that we have with us, is communicated over the world using some techniques. The data we send are in the form of bits or binary values (as 0s or 1s). To make the transmitting data robust, efficient and accurate we use some encoding/decoding techniques. One such coding technique is the 'Manchester coding' which comes under Digital Line Encoding and Decoding techniques that are widely used in Industrial applications. The transmission of data through communication buses and networks are generally in the form of binary digits (i.e. 0's and 1's). To avoid the DC term in the transmitting signal we are going for Manchester which makes a transition at the middle of each bit. This paper deals with the implementation of a Manchester Encoder and Decoder circuit along with invalid detection and clock recovery unit (CRU) using HDL (Hardware Description Language). This encoding technique is widely used in fields like Satellite Communication, Bio-medical applications, Servo systems, Magnetic recordings etc.

1. Introduction

The network is used for the communication of data from one station to another station. This can be through a physical (guided) medium where there exists solid path between the sender and the receiver or non-physical (un-guided) medium where no solid path exists. The analog or digital data to be transmitted, travel through a communication media in the form of a signal. But, irrespective of the medium, the signal travelling through the channel becomes attenuated and distorted as the distance increases. Hence a technique must be adopted so that the transmission of data happens, such that the properties of the data signal and that of the transmission media will match; there by providing an efficient communication over the transmission media. There are two alternatives; the data can be either converted to digital or analog signal. What to be used depends on the situation and the available bandwidth and the source signal. One such digital coding technique is the Manchester Encoding/Decoding.

2. Manchester Encoding and Decoding

Manchester Coding is a common technique which comes under the Digital Data Coding. The term coding includes both Encoder and Decoding. Purpose of an Encoder is to convert the bits or data into a coded data and that of the Decoder is to recover the original data from the coded form. The Encoder is used along with the transmitter and the Decoder along with the receiver. Here each interval is divided into two halves. Therefore there will be a change of signal level at the middle of each bit.

A Rise transition (Low to High transition) at the input side corresponds to a binary One ('1') and a Fall transition (High to Low transition) corresponds to a binary Zero ('0'). Because of the transitions at the mid of the bit, there is no chance of occurrence of DC signal, i.e. continuous Zeros and Ones.

3. Encoder Implementation

The function of Manchester Encoder is realized using Combinational circuits. The design of the Manchester Encoder is shown in the Figure. 1 using three AND and one XOR gate.

Table 1. Truth Table for Manchester Encoder

CLOCK	ACTIVE	ACTIVE	ACTIVE	ACTIVE	ACTIVE
DATA	0	1	1	0	1
BITS	10	01	01	10	01
TRANSITIONS	HL	LH	LH	HL	LH

The implementation is done using four logic gates. Function of Gate 1 is for clock gating. Gate 2 is for the ex-or operation of the data and the clock signal.

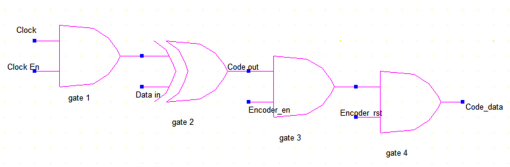

Figure 1. Circuit of Manchester Encoder

Gate 3 and Gate 4 forms the control circuitry for Reset and Encoder enable operation. The final output code_data will be in the form of High and Low transitions. The designed encoder can intake 8 bit serial data and corresponding to each bit, it codes and form the transitions.

4. Decoder Implementation

The function of Manchester Decoder is realized using Combinational and Sequential circuits. Combinational circuit includes logic gates for Reset and enable control actions along with the ex-or operation for the Clock recovery. The sequential circuit includes latches and flip flops for the transition detection function for Data recovery. This is designed without any input clock signal so that it can work at any data frequency. The basic block diagram of the Decoder unit is shown in Figure 2. First the Recovery of data must happen and depending on the recovered data and incoming code, we are recovering the clock signal.

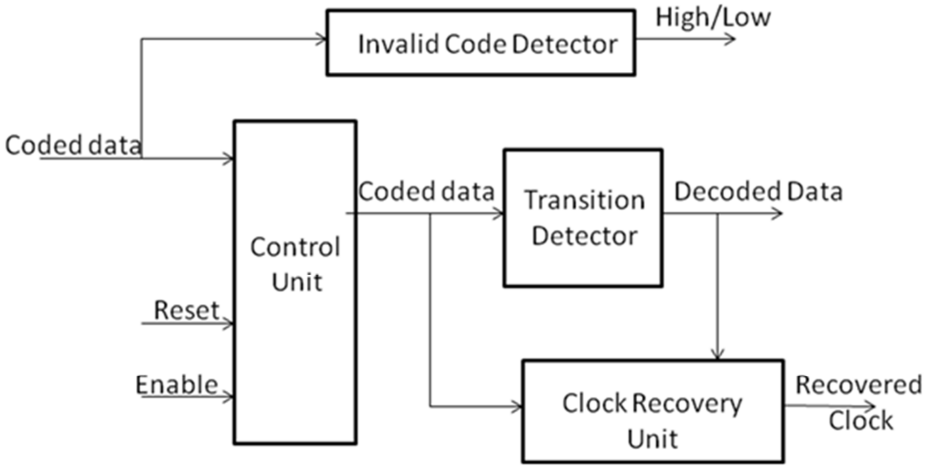

Figure 2. Block Diagram of Manchester Decoder circuit

An additional circuitry is also provided which is used to detect the invalid code at the input. This unit will generate a High output signal whenever an invalid input comes and will generate a Low otherwise. This performs by continuously analyzing the state of the input code data.

5. Simulation Results

The programming of the Manchester Encoder and Decoder is done using Verilog Hardware Description Language and the simulation is done using Modelsim 6.4SE software. The simulation result of the Manchester Encoder is shown in Figure 3.

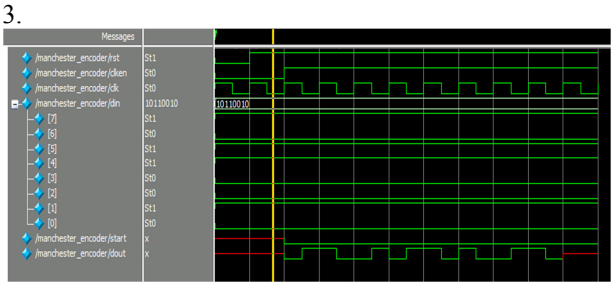

Figure 3. Simulation result of Manchester Encoder with a clock having 50% Duty Cycle

The input signals are the Clock, Clocken, Reset and the input data to be coded. The whole data to be coded comes in parallel format. The data is first serialized and then taken for encoding operation. The output bits are the Start bit which will be High at the converting stage and Low after conversion. Dout gives the Encoded output. The simulation result of Encoder with different clock frequency is shown in Figure 4.

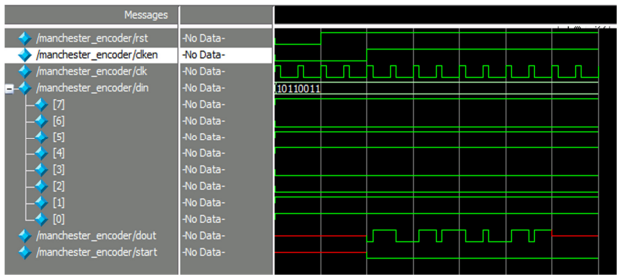

Figure 4. Simulation result of Manchester Encoder with a clock having 25% Duty Cycle

The simulation result of Manchester Decoder is shown in the Figure 5. The input and Output signals are declared as bits.

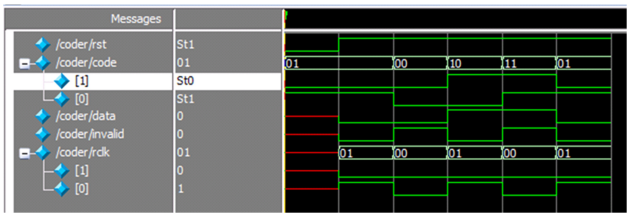

Figure 5. Simulation result of Manchester Decoder

The input code is given as bits. ‘01’ indicates a Low to High transition and ‘10’ indicates a High to Low transition at the input. ‘00’ and ‘11’ indicates invalid inputs which are a steady low and steady high signal respectively. The recovered clock is also shown in the form of bits. ‘01’ indicates the correctly recovered clock with a Low to High transition and ‘00’ indicates no recovery of the clock signal.

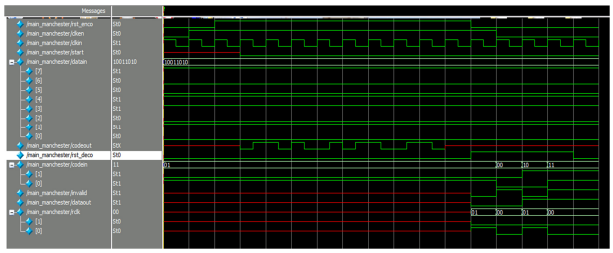

Figure 6. Simulation result of the top module of Manchester Encoder/Decoder

Figure 6 shows the simulation of Manchester top module including both the encoding and the decoding functions. During the working of Encoder, the Decoder will be in a disabled state and during the working of Decoder, all the output signals of encoder will be zero.

6. Conclusion

The main advantage of this work is that the implementation is done using Combinational and Sequential circuits which makes the design simpler, robust and easy to design. Also a combined implemention of the circuit is provided including Manchester Encoder and Decoder along with Invalid code detector and Clock recovery unit (CRU).

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