

# Implementation of Full Adder Circuit using Stack Technique

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## Abstract

This paper presents a design of a one bit full adder cell based on stack effect using Double Gate MOSFET. This design has been compared with existing one-bit full adder which is designed using power gating technique. In this paper, the proposed circuit has been analyzed for parameters like- power consumption and power delay product. The simulations of the proposed Full Adder have been performed using Tanner EDA Tool version 16.1. All the proposed design simulations are carried out at 45nm technology for various inputs like supply voltage and input voltage. The decrease of 91.1% in power utilization has observed in proposed circuit. The results show a legality of double gate MOSFETs for designing for low power full adder circuit.

**Keywords:** DG-MOSFET, ALU, XOR, Full Adder, PTI, GDI, Diffused Gdi, Finfet, ELK, Power Grating, Stacking.

## 1. Introduction

Electronic devices such as mobile phones, cameras are used commonly these days. Its battery life span is of great concern. When mobile phone is operated in standby mode, certain programs of mobile phone or camera are turned off during active or talk mode but this doesn't stop the battery from getting depleted. This is because circuits which are de-activated by turning off certain programs still have leakage currents flowing through them. Even though the magnitude of leakage current is lesser than the normal operating current but leakage current erodes battery life over relatively long standby time whereas the normal operating current erodes battery life over relatively short talk time. Thus this is why low power circuits for mobile applications are of great interest. Implementation of adder cells to reduce the power consumption and to increase the speed has proved to be a worthy solution towards power reduction. Moreover, realization of adders with different approaches using CMOS technology widens the area of power reduction, performance of the adder cells can be evaluated by measuring the factors such as leakage power, active power in context to voltage and transistor scaling. Reducing transistor gate length when no voltage is applied at gate results in more leakage current between source and drain of the transistor. Eventually results in the more power consumption in microprocessors and digital signal processors. In general, a one-bit full adder core has three inputs ( $A$ ,  $B$ , and carry in  $C_i$ ) and two outputs (sum  $S$  and carry out  $C_o$ ). The complex arithmetic circuits such as subtraction, multiplication, and division functions usually can be realized by co-operations of multiple adders. An adder performance affects the arithmetic system as a whole. There are two major methodologies to improve adder's performance in the state-of-the-art research. One is 'architecture viewpoint' approach, which is, finding the longest critical paths in the multi-bit adders and then shortening the path to reduce the total critical path delay. In most cases, the longest signal path exists in propagation of carry out signals to generate the carry out signal of the most significant bit (MSB). The other approach is 'circuit design viewpoint' in transistor level, that is, design of high performance full adder core based on transistor level design skills as shown in Figure.1(a). Commonly, many design considerations including the minimum transistor counts, low power consumption, high throughput, full-swing output, driving capability, chip area, and layout regularity are focused recent [Ravindra Singh Kushwah, Shyam Akashe,(2013)].

Furthermore, more and more portable devices are commonly used today. The mobile computer, cellular phone, and laptop devices not only need low-power consumption but also high-speed. A world without electronics cannot be imagined in the present generation. The use of electronic items has encompassed our regular work day to such a degree that it is impracticable to spend a few hours without them. At the outset of the day to its end, we use a battalion of electronic gadgets to enhance various problem solving activities. In sum, we are very dependent on the electronics, as they facilitate our day to day lifestyle. For example, the use of mobile phones has changed the definition of communication. The Smartphone was introduced to the public in 1993, with added features like: gaming, email, etc. Instead of physical buttons, the users touch the screen to select the required options. Researchers found that its usage has had a rapid increase from the year 2006 till present. According to a recent survey, 77 percent of the world population uses the mobile phone. Also we use a variety of portable electronic devices which are inbuilt with a variety of operating systems. It is difficult for us to imagine the world without electronic devices. The main difference between a half-adder and a full-adder is that the full-adder has three inputs and two outputs. The first two inputs are  $A$  and  $B$  and the third input is an input carry designated as  $C_{IN}$ . When full adder logic is designed we will be able to string eight of them together to create a byte-wide adder and cascade

the carry bit from one adder to the next. The output carry is designated as COUT and the normal output is designated as S[Massimo Alioto and Gaetano Palumbo,(2002)].

From the truth-table I, the full adder logic can be implemented. We can see that the output S is an EXOR between the input A and the half-adder SUM output with B and CIN inputs. We must also note that the COUT will only be true if any of the two inputs out of the three are HIGH. Thus, we can implement a full adder circuit with the help of two half adder circuits. The first will half adder will be used to add A and B to produce a partial Sum. The second half adder logic can be used to add CIN to the Sum produced by the first half adder to get the final S output. If any of the half adder logic produces a carry, there will be an output carry. Thus, COUT will be an OR function of the half-adder Carry outputs. Mostly used to represent the operation. Given below is a simpler schematic representation of a one-bit full adder is shown in Figure. 1(b).

With this type of symbol, we can add two bits together taking a carry from the next lower order of magnitude, and sending a carry to the next higher order of magnitude. In a computer, for a multi-bit operation, each bit must be represented by a full adder and must be added simultaneously. Digital Signal Processing (DSP) is commonly used in devices such as mobile phones, laptops, multimedia computers, camcorders, CD players, hard drives etc. A DSP chip is a programmable device, which has a set of instructions that enable various algorithms to be coded into it. The adder is one of the key components of a DSP chip. Recent devices like microprocessors have become quite powerful with the ability to perform millions of operations per second. As the number of transistors on a chip increases, the power consumption becomes a concern especially for use in portable electronics. The tremendous demand for the low power and high performance designs has grown significantly in recent years and this has been due to the fast growth of battery operated portable devices. Further, the aggressive scaling of transistor size for high performance applications necessitates the integration of new device structures. The Double Gate MOSFETs are example of this, which are capable for nano-scale integrated circuits. Double Gate MOSFET (DG MOSFET) is widely used in ultra-low power design. When devices are scaled, leakage and short channel effects (SCEs) such as the sub threshold slope and the drain induced barrier lowering (DIBL) became prominent[Anuj Kumar Shrivastava1, Shyam Akashe, (2013)]. The front and back gates are electrically coupled together in Double Gate devices and this reduces the short channel effect and sub threshold leakage. The use of two gates leads to the increase in current driving of Double Gate and hence the circuit with Double Gate transistor can be operated at much lower input and threshold voltages compared to Existing circuit MOSFET circuit and these means lower power consumption. The intimate coupling between the gates and the channel makes DG MOSFET technology the most scalable of all MOSFET designs. Due to the presence of two gates, no part of the channel is far away from the gate. The voltage applied on the gate terminals control the electric field, determining the amount of current flow through the channel. This gives the ideal sub threshold slope for sub threshold operation. Because of better control on short channel effect, Double Gate MOSFET is used for sub threshold circuit design. Sub threshold circuits operate with a supply voltage less than the threshold voltage of the MOS transistor. The use of sub threshold circuit designing in fast and energy efficient circuits is always needed in electronics industry especially in DSP, image processing and arithmetic units in microprocessors. Addition is the most basic arithmetic operation and adder is the most fundamental arithmetic component of the processor. Thus, it is worthwhile design a full adder cell with DG MOSFET and study the behavior we obtain moving towards Double Gate technology. The Figure.1 (c) shows symbol of double gate MOSFET and Figure. 1(d) shows a symmetrical and asymmetrical mode of operation of double gate MOSFETs. The paper is organized into five sections. Section I give the general information for low power designing and introduce DG-MOSFET device. Section II illustrates the existing full adder cell as reported in the literature. In, section III full adder cell using DG MOSFET has been proposed. Simulations, results and comparison are given in Section IV and finally Section V concludes the paper[Amara Amara, Chetan D. Parikh and D. Nagchoudhuri,(2011)], [H.-S. P.Wong,(2001)].

## 2. Design of existing

1 bit full adder In this paper we designed full adder with the help of double gate transistor, the used parameters value has been varied significantly thus improving the performance of full adder. Power Gating is one of the most used circuit techniques to reduce the leakage current in idle circuit. In this paper different parameters are analysed on Power Gating Technique. Simulation results of double gate full adder have been performed on cadence virtuoso with 45nm technology.

Full adder is a combinational circuit that performs the addition operation of input bits. Full adder basically consists of three inputs and two outputs. The input variables are denoted by A, B and Cin. The two output variables are denoted by sum(S) and carry (Cout). shows the basic block diagram of full adder cell. The Boolean expression for full adder operation is

Figure.2(a) shows the double gate 10T full adder circuit. This adder circuit is constructed by using the 4T XOR gate. XOR gate is the basic element of full adder cell and generates the basic addition operation of adder cell. It behaves like a single half adder cell. Conventionally XOR gate use 8 MOSFETs for proper working, topologies. Here we have used 4T XOR gate to increase circuit density. The 4T XOR gate. Reduction in size of full adder is

achieved by using this XOR gate and overall leakage is also reduced.

### 2.1 Power gating technique

Power Gating, it reduces the leakage by inserting n- MOS and p-MOS to the circuit. Fig. 6 shows the Power Gating circuit. This technique is very widespread for reducing leakage in the circuits. Because of the easiness of execution of the technique, power Gating has been used to minimize. Leakage energy in circuits at the architectural level [Ruchika, Tripti Sharma and K. G. Sharma,(2014)] [A. K. Shrivastava and S. Akashe,(2013)]. The power gating is shown in Figure.2 (b).The effectiveness of power gating required following:

- It provides the switches for turning off and on of the functional units at circuit level.
- These switches controls the power gate at various parts of the circuit can be provided as handles at the system software or the level thereby giving the system compiler the ability to control them.

The simulations are done using SPICE tool in a 45 nanometer (*nm*) standard CMOS technology at room temperature; with supply voltage of range of 0.3- 0.7 at 100 MHz frequency. The input and output waveforms show that this circuit works perfectly as full adder circuit and have very less degradation in outputs of this circuit. The waveforms are shown in Figure.2 (b). The simulations show following results for power consumption and power delay product. The average power consumption and pdp is 7.265 and 1242.315 respectively.

### 3. Proposed full adder

DG- MOSFET full adder circuit has been designed using the equivalent style. The full adder circuit using Double gate MOSFET has been shown in Figure.3 DG- MOSFET will be constructed by connecting two single gate MOSFET transistors in parallel in such a way that their source and drain are connected together. The schematic of full adder is implemented using double gate MOSFET in symmetrical driven mode. There are number of adder circuits have been designed using DG-MOSFETs [Shipra Mishra, Shelendra Singh Tomar, Shyam Akashe(2013)]. The proposed adder circuit consists of 10- transistors and called as 10-T adder cell. The proposed circuit is implemented using three main components, namely XOR, inverter, and Multiplexer. To reduce the leakage current in the circuit, a stack pMOS transistor is added into one of the inverter. The proposed circuit is simulated for total power consumption and delay. When the inputs  $A=B=0$ , the XOR gate will introduce  $1-V_t$  loss and this loss causes the nMOS transistor (N1) of the inverter not to be completely turned off (weak inversion) and results in subthreshold leakage current. The subthreshold leakage current causes higher power dissipation in the circuit. To avoid this leakage current problem, we have introduced a pMOS (Pstack) transistor in series with the pull up transistor of the inverter.

This extra transistor gives lower leakage as well as ensures that pull up pMOS is completely off when either inputs (A or B) are high. The added transistor will slightly degrades the response of carry-out because pMOS is slower device. Subthreshold current depends exponentially on  $V_t$ ,  $V_{DS}$  and  $V_{GS}$ . Therefore it is a function of the terminal voltages,  $V_D$ ,  $V_B$ ,  $V_S$  and  $V_G$ . This means that to know subthreshold leakage of a device the biasing condition should be known or by controlling the terminal voltages the subthreshold leakage can be controlled. Input pattern of each gate affects the subthreshold as well as gate leakage current. The leakage of transistors in a stack is a function of no. of transistors and input pattern. Source biasing is the general term for several techniques that change the voltage at the source of a transistor.

The goal is to reduce  $V_{GS}$ , which has the effect of exponentially reducing the subthreshold current. Another result of raising the source is that it also reduces  $V_{BS}$ , resulting in a slightly higher threshold voltage due to the body effect. Circuits that directly manipulate the source voltage are rare, and those that exist usually use switched source impedance or a self reversed biasing technique Probably the simplest example of source biasing occurs when “off” transistors are stacked in series. Conceptually, the source voltage of the upper transistor will be a little higher than the source voltage of the lower transistors in the stack. Hence  $V_{GS}$  of upper transistor is negative,  $V_{BS}$  is negative resulting in increase in threshold voltage and  $V_{DS}$  is also lower. Due to this, the leakage of upper transistor reduces. This reduction is called stack effect. The proposed circuit shows better output waveforms at lower input voltages. According to the DG- MOSFET, the chip area of a p-type DG MOSFET and n-type DG MOSFET are same, and the amounts of current related to them can also be the same. The W/L ratios of transistors are taken as 5/1.

### 4. Simulation results for proposed circuit

The simulations of proposed circuit have been done at 45 nm using level-54. The transient analysis has been performed for different input voltages, temperatures and frequency. The output waveforms of proposed circuit have been shown in Figure. 4(a). The variation of power consumption and power delay product with respect to input voltage respectively is observed keeping other parameters like frequency and temperature constant. The average power consumption and PDP for existing circuit is given as  $4.23 \times 10^{-8}$  W and  $80.505 \times 10^{-18}$  respectively. The average power consumption and pdp is 58.22 nW and  $55.17 \times 10^{-18}$  respectively for proposed circuit as shown in Table IV and V respectively. The table VI reveals 91.1% Decrease in Power consumption reduction in power

consumption in proposed full adder. The Table VII shows comparison of power delay product with respect to input voltage and it is observed that there is 18% reduction in PDP. This shows the superiority of proposed DG-MOSFET full adder circuit for ultra low power designing.

## 5. Conclusion

In this work we designed the double gate 1 bit full adder. Double Gate MOSFET technology achieves low leakage and high performance operation with high speed. The double-gate (DG) or multigate devices provide a better scalability option due to its excellent immunity to SCEs [9]. We have studied various full adder circuits and conclude suitability of DG MOSFETS for them. Different parameters are analyzed at various voltage supplies. Simulation results of double gate full adder have been done in Tanner tool at 45 nm technology. The power consumption gets worst with increasing the power supply. The power delay product is increased with supply voltage due to scattering effects at higher temperatures. The proposed circuit can also work for wide range of input voltage. New full adder is implemented using stack effect. The results showed that proposed 10T full adder circuit shows power is 91.1 % less than base circuit. Further PDP is reduced by 18%. The proposed circuit shows overall improvement in terms of power dissipation and power delay product. Further this full adder circuit can be used for various electronic and digital circuits. It can be used for implementing digital signal processors, arithmetic logic units and etc.

## Acknowledgment

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References

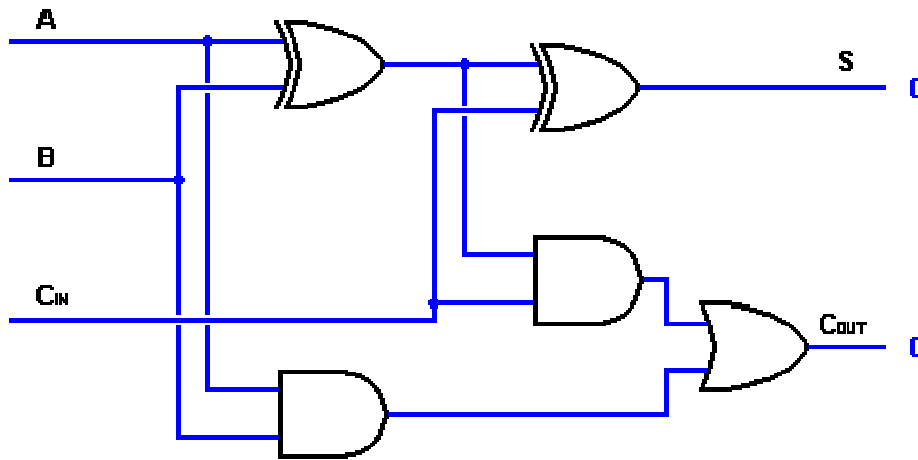


Figure.1(a) Full Adder Circuit

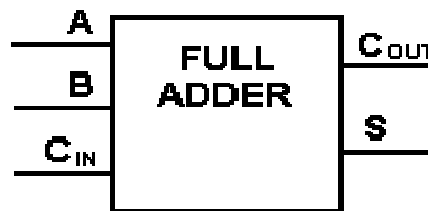


Figure.1(b) Single-bit Full Adder

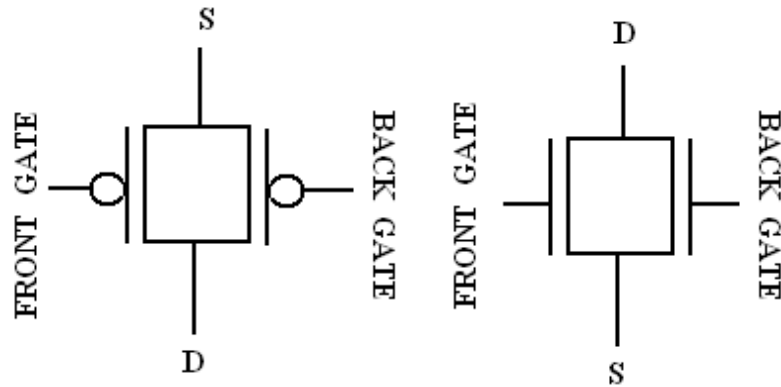


Figure.1(c). Circuit symbols for p-type and n-type DG- MOSFET transistor

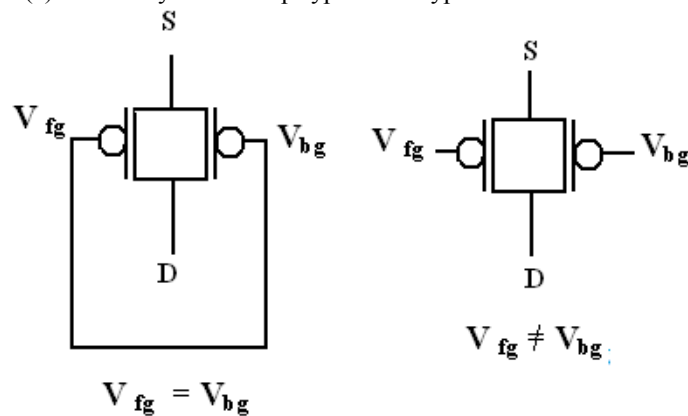


Figure. 1(d). Symmetrical and independent driven double gate MOSFETs

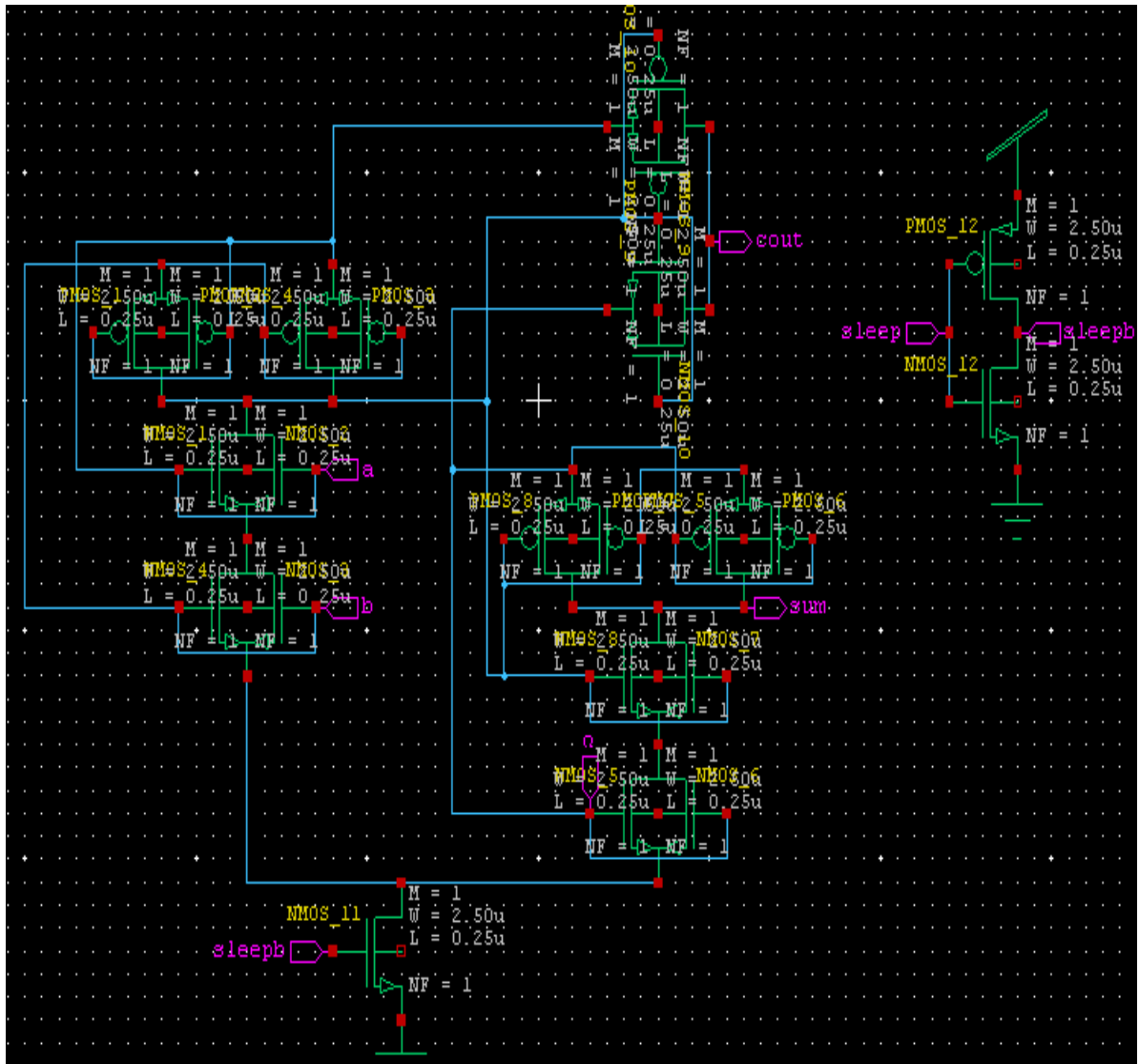


Figure. 2(a) Existing full adder with Double Gate

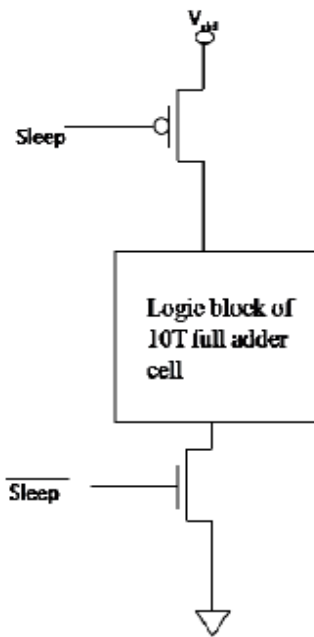


Figure. 2(b) power gating technique

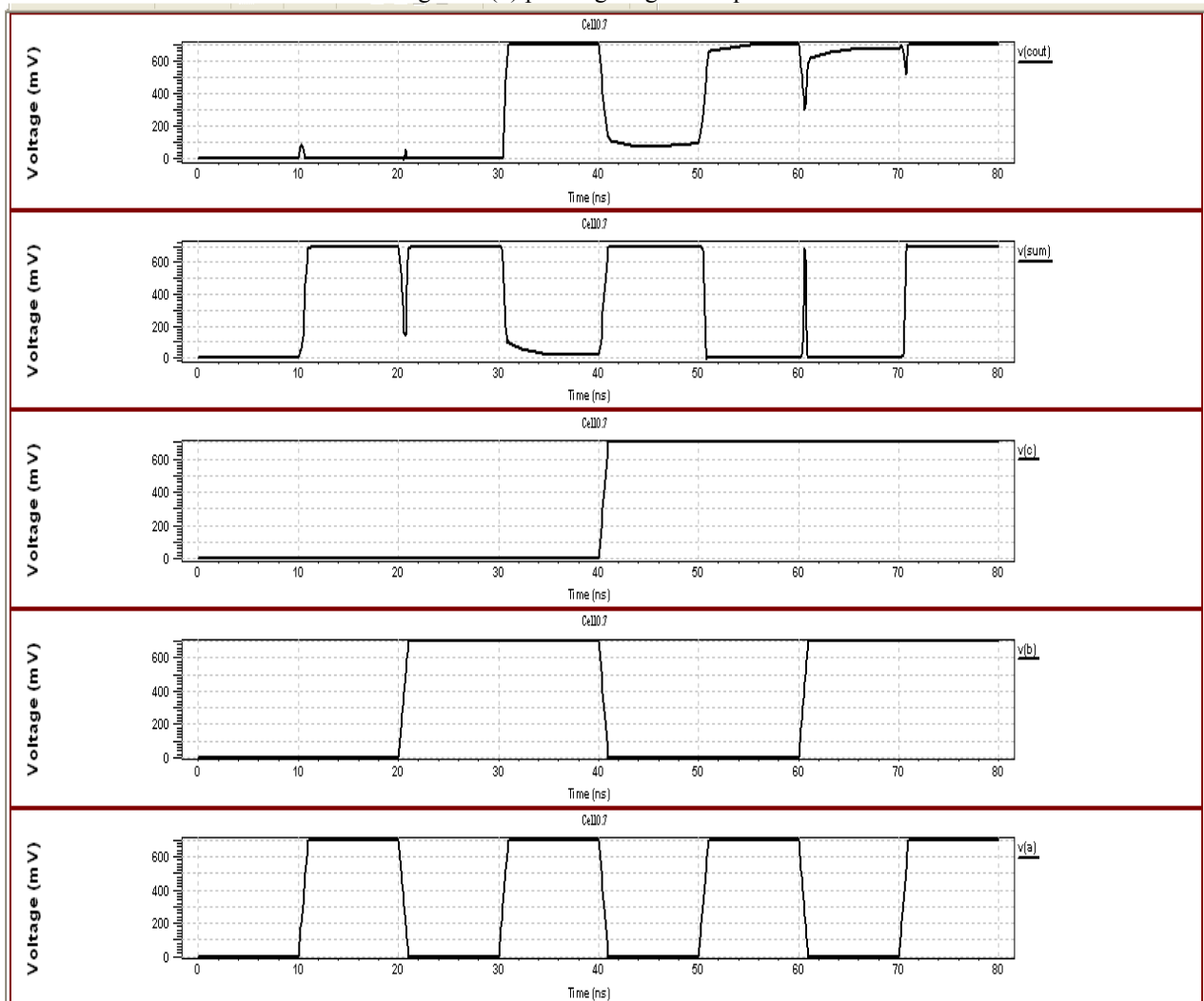


Figure. 2(c) . transient Analysis for existing full adder

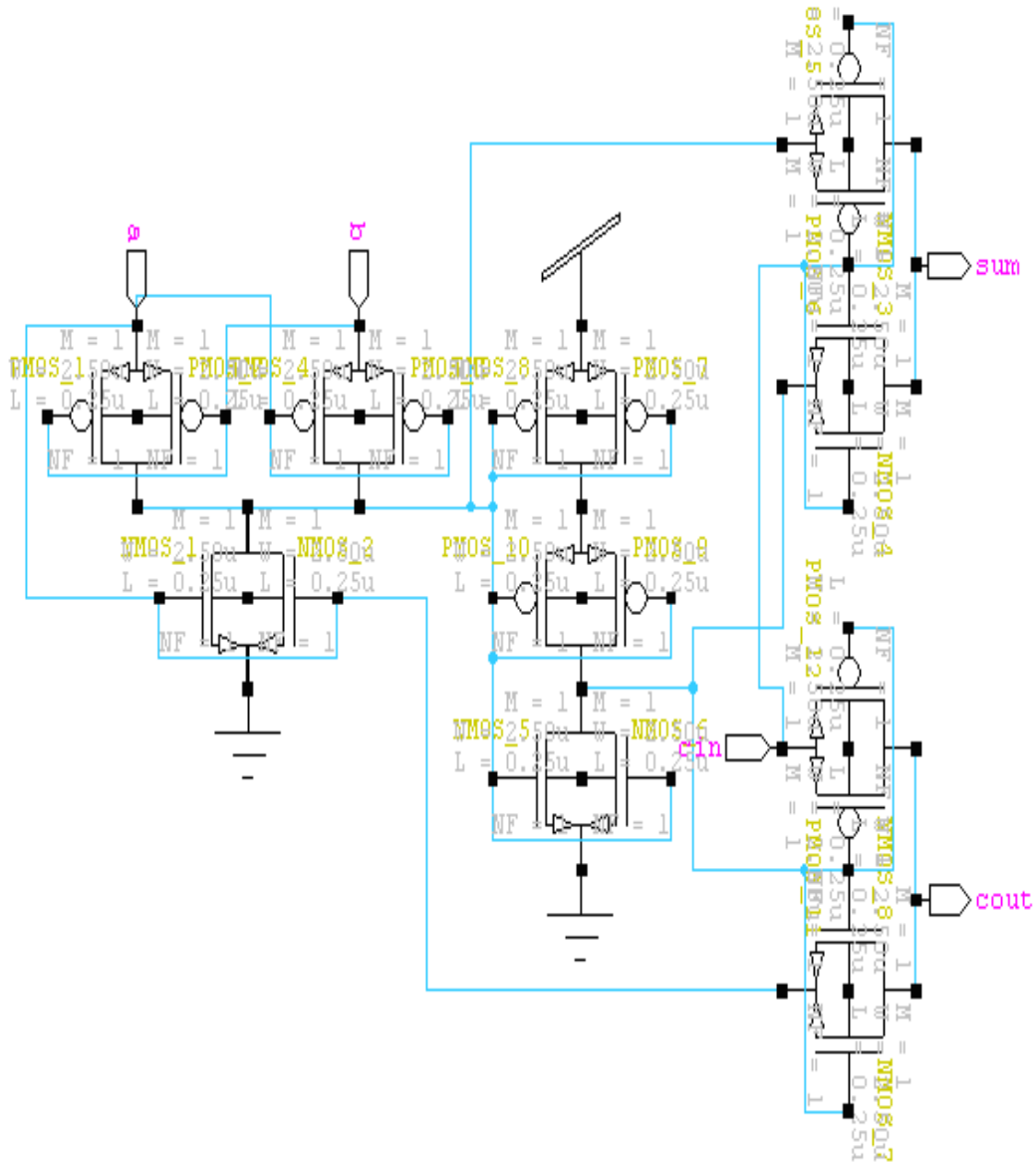


Figure.3(a) proposed Double Gate Full adder



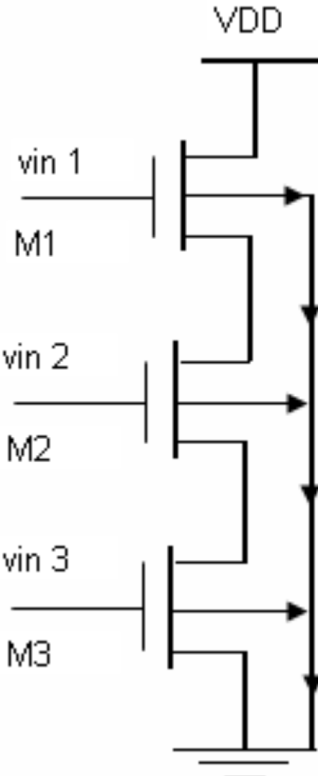


Figure.3(b) stack effect

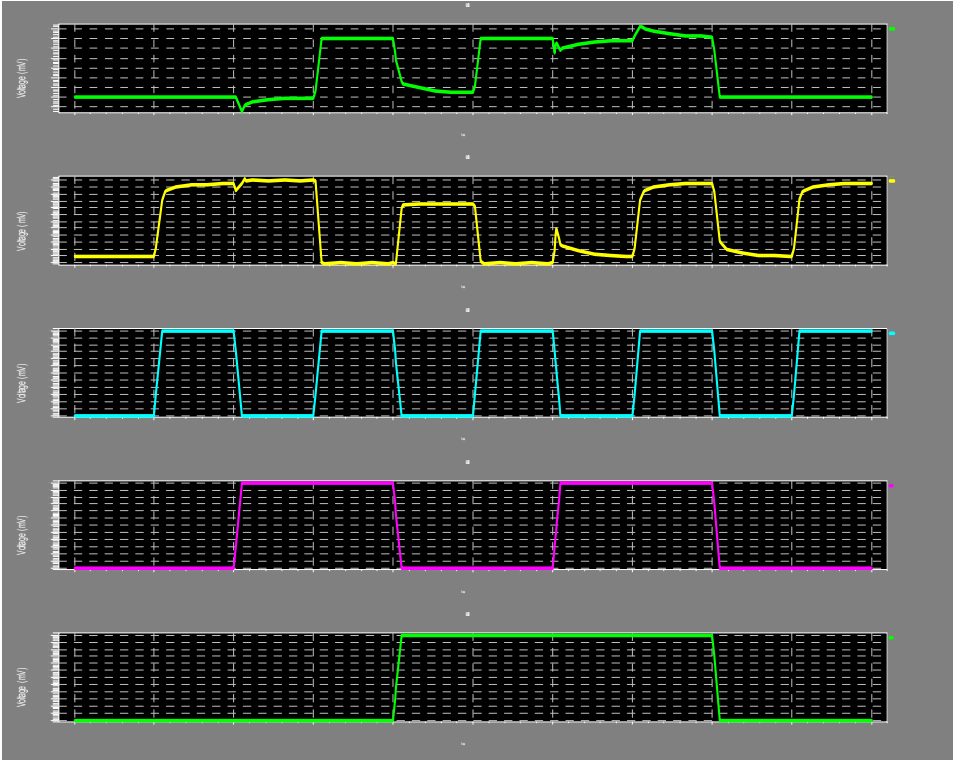


Figure 4(a). Transient analysis for proposed circuit

Table I Truth Table for full adder

a	b	c	sum	carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1

Table II power consumption with input voltage for existing circuit

Sr. no.	INPUT VOLTAGE (in V)	POWER CONSUMPTION (in W)
1	0.3	3.245 e-008
2	0.4	3.605 e-008
3	0.5	4.87 e-008
4	0.6	5.22 e-008

Table III: pdp with input voltage for existing circuit

INPUT VOLTAGE (in V)	POWER DELAY PRODUCT (in e-18)
0.3	67.89
0.4	80.34
0.5	84.45
0.6	89.34

Table IV: power consumption with input voltage for proposed circuit

INPUT VOLTAGE ( V)	POWER CONSUMPTION ( nW)
0.3	30.45
0.4	56.90
0.5	67.09
0.6	78.45

Table V: pdp with input voltage for proposed circuit

INPUT VOLTAGE (in V)	POWER DELAY PRODUCT ( e-018)
0.3	45.89
0.4	48.90
0.5	57.34
0.6	68.56

Table VI: comparison for power consumption for existing and proposed circuit

<b>INPUT VOLTAGE (in V)</b>	<b>POWER CONSUMPTION Existing Circuit (in W)</b>	<b>POWER CONSUMPTION Proposed Circuit (in W)</b>
0.7	7.265 e-008	7.9611 e-009
0.8	11.05 e-008	8.1994 e-009

Table VII: comparison for pdp for existing and proposed circuit

<b>INPUT VOLTAGE (in V)</b>	<b>POWERDELAY PRODUCT Existing Circuit (in e-18)</b>	<b>POWERDELAY PRODUCT Proposed Circuit (in e-18)</b>
0.7	92.45	76.45
0.8	100.45	80.34