Design of SRAM Cell Using DG-MOSFETs at 45 nm Technology

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Abstract
As the technology in electronic circuits is improving, the complexity in these circuits also increases. The complexity in the circuits leads to the need of that type of circuits which are portable and fast circuits. The portability in the electronic circuits is achieved by the use of battery. So we have to develop such sort of circuits that use very less power. The main focal point in designing a high performance digital system such as microprocessors and various Digital signal Processors is given to low power design. The key part of any digital system is its memory unit. It is not possible to design a digital system without memory. So we can say that memory is the main part which employ the highest power in the system. The most used memory cell in the digital systems is the SRAM cells. They are the static RAM cells. Low-power Random Access Memory (RAM) has seen a remarkable and rapid progress in power reduction. The high density and low power SRAMs are needed for application such as hand held devices, laptops, notebooks, IC memory card because of the fact that they are portable devices and uses batteries for power source so they must consume power as low as possible. As the semiconductor technology scales down, the read stability and write capacity of a static random-access memory (SRAM) cell are degraded because of the increased mismatch among its transistors. In sub-threshold conduction, leakage current is main culprit to increased power dissipation and degradations. There are scale issues which arise in nanometer range of operation. These issues cannot be resolved in conventional MOS transistors. DG-MOSFETs are one of the attractive candidates to reduce these problems in extremely nano-scaled devices. Further SRAM cell are chief component for today's electronic industry. This report presents a novel CMOS four and two-transistor SRAM cell for very high density and low power embedded SRAM applications as well as for stand-alone SRAM applications.
Keywords:SRAM, Tanner 16.0, 4T&2T SRAM Cell

1. INTRODUCTION

This paper a presents designs of SRAM a memory cell. SRAM [(Ajay Kumar Dadoria, Arjun Singh Yadav, 2013)], [(Abhishek Kumar),2014]parts take become an important block in modern SoCs. The collective number of transistor sum in the SRAM units or the surging leakage current of MOS transistors in the scaled tools have complete the SRAM part a power voracious block from mutually dynamic and static outlooks. Remaining to high bit line voltage swipe during compose the operation, the write power depletion is controlled the dynamic power consumption. The fixed power consumption are mainly due near the leakage current connected with the SRAM cells circulated in the array. Besides, as supply voltage losses to throw the power depletion, data constancy of the SRAM cells have become a major distress in the recent years. Now reduce the silicon area or to realize high speed and performance, devices are being scaled down to the great level. To Supply voltage or size of the transistors are most significant factors these are only factors in the hand of the design engineer. Normally supply voltage is scaled down to less the static power degeneracy, then along by that for high performance of the thresholdvoltage must also be scaled down. The decrease the threshold voltage different phase increases the associate threshold leakage current which leads near increment in the static power dissipation. Fixed power dissipation is essentially contributed in sub threshold current or gate leakage current. The hide memory in the microprocessor inhabits more than 50% of chip area hence the leakage power of hide is a main source of power dissipation in to the processor. For reliability of the SRAM cell still voltage noise margin (SVNM), static current noise border (SINM), write trip voltage (WTV) and write trip current (WTI) is the most essential parameters to the memory design. Total leakage power in SRAM cell is determined by the impact of leakage currents individually the transistor of SRAM cell. The leakage current takes two main sources, sub-threshold leakage current or gate leakage current (leakage current is controlled by sub-threshold leakage).The band to band excavating leakage current is very less for present Technologies 90 nanometer or that can be ignored . Equally to the oxide depth of gate decreases, gate leakage current of the transistor increases exponentially or when gate oxide thickness extents 3nm and below, the gate leakage current comes to the demand of subthreshold leakage current. It also growths exponentially with voltage through gate oxide.The name static, means that the memory recalls this contents the long as the power are turned on. Random access funds that locations in the memory be able to be written to or read from in some order, irrespective of the memory location that was last the accessed. Each bit in an SRAM is the stored on four transistors that form two cross-coupled inverters. Its storage cell has two steady states which are used to symbolize "0‟ and "1‟. The access transistors are used to access to the stored bits in the "SRAM" through read and write mode. The conventional SRAM cell use to take 6 MOSFET to the store one memory bit. The SRAM Cell is Memory cells are the key components of any SRAM part. The SRAM cell be able to store one bitof data. A SRAM cell comprises 2 back-to-back connected inverters making a latchand two contact transistors. The Access transistors serve for read or write access the cell. A number of SRAM [(Vijay Singh Baghel and shyam akanskhe, 2015)], [(K. Shrivastava and S. Akashe), 2013] cell topologies have been reported in the older decade. Between these topologies, resistive capacity four-transistor 4T cell, load less (4T) cell or the six transistor 6T, SRAM cell consume received attention in the practice, owing to their balance in storing logic `1' and `0'.

2. DOUBLE GATE

Silicon Technology is used to electronics devices like cellular phones, game consoles, personal computers, and super-computers are a few examples. Large growth in silicon technology havemade possible to construct smaller transistors and complex integrated circuits. Downscaling of CMOS technology [(John P. uyemura), 2007], [(SUNG-MO (STEVE) KANG&YUSUF LEBLEBIGI), 2006] with improved RF figures-of-merit has made it attractive for system-on-chip applications. The market demand for energy-constrained battery operated and smaller size devices has tremendously increased. Apart from smaller size, the operating speeds and low power consumption of devices is the demand of the day and the future of digital devices. Therefore, the design of devices and circuits for such ultralow-power applications is a challenging task. The semiconductor industry has reached to nanometer era according to the International Technology Roadmap for Semiconductor (ITRS) [(John P. uyemura), 2007]. This has led to device gate-lengths.

The symmetric nature in a reduces the depletion-width by 50% compared to that of a single-gate structure The double-gate (DG) or multigate devices provide a better scalability option due to its excellent immunity to SCEs. Among the other advantages of DG MOSFETs are the near 60 mV/dec subthreshold slope, the low drain-induced barrier lowering (DIBL), and the possibility of using a lightly doped or an undoped body. Most of the research studies on DG as shown in Figure1 architecture were carried out in the field of logic applications.This work, we have described the device structure of DG-MOSFETs, and its suitability to make radio frequency devices. The back gate will be used for the tuned circuit performance. Due to analog tunable functionality, these circuits provide extra gains in terms of area, power and speed by using DG-MOSFET in independently driven mode (IDDG) where the two gates are separated and biased in a different way as compared to symmetrically driven mode (SDDG) counterparts used in digital applications to maximize I_{ON}/I_{OFF} ratio. We conclude that The DG devices can be used to improve the performance and reduce the power dissipation when front gate and back gate both are independently controlled.

3. PROPSED CELL ARCHITECTURE

A. Schematic 4T & 2T SRAM Cell

In this chapter, we have proposed 4T and a 2T SRAM as shown in Figure 3 and 4 respectively circuit which shows better results as compare to given circuit. DG- MOSFET 4T and 2T SRAMs circuits have been designed using the equivalent style. The schematic circuit using Double gate MOSFET has been shown in Figure.2 for 4T SRAM circuit. DG- MOSFET will be implemented by connecting two single gate MOSFET transistors in parallel in such a way that their source and drain are connected together. The two gates in DG-MOSFETs lead to increased current driving property of transistor. The DG-MOSFET structure provides electrostatic coupling for conduction channel and two gates allows additional gate length scaling by factor of 2 as compare to the single gate MOSFET [(Younghwi Yang, Juhyun Park, Seung Chul Song, Joseph Wang, Geoffrey Yeap, and Seong-Ook Jung),2015]and . The schematic of single gate MOSFET based SRAM circuits are implemented using double gate MOSFET in symmetrical driven mode. There are many memory circuits have been designed using DG-MOSFETs. The proposed circuit shows better output waveforms at lower input voltages. According to the DG- MOSFET, the chip area of a p-type DG MOSFET and n-type DG MOSFET are same, and the amounts of current related to them can also be the same. The W/L ratios of transistors are taken as 1/1.

B. Simulation Results and Analysis at 45nm for 4T and 2T SRAM

The circuit is simulated at 45 nm using BSIM3 V3 on tanner EDA tool. The results are compared at this technology length and analyzed the effect of decreasing feature size on results of these SRAM circuit. The output waveform for write and read cycle is shown in Figure 4and 5 respectively. Power Results for write cycle is 3.857758e-008 watts and Pdp observed is 361 e-18 watt-secs for 4T. Power is reduced as w/l ratio is reduced with technology. For 4T, Power Results is 40 nwatts. Pdp observed for this circuit is 364 e-18the simulation results for 2T SRAM cell at 45 nm technology. Figure 6 and 7 presents output results for write and read cycle for proposed 2T SRAM cells and Power Results for write and read cycle for 2T is 110 nwatt and 154 nwatt respectively. The pdp is 1.254 e-15watt-sec and 1.590 e-15watt-sec for write and read respectively.

4. CONCLUSION

With the aim of achieving a high-density SRAM, we developed a 4T and 2T SRAM cell using DG-MOSFETs. DG-MOSFETS are new emerging transistors which can work in nanometer range of operation. The simulation of existing as well as the proposed cell has been performed according to the parameters shown in Table-1. The proposed SRAM Designs are purposed to realize to consume less pdp as well less power compared to previous existing design. Analytical results show, on average novel 4T and 2T SRAM cells have 99% smaller dynamic Power consumption. The Simulation result are done in standard 45 nm CMOS technology shows purposed 4T and 2T SRAM cell has correct operation during read/write operation and idle mode. 2 T SRAM circuits have higher power consumption and pdp as compare to 4T but since number of transistors are reduced by 50%. We have to take a tradeoffs and parameters under consideration for particular design. Further we can use these purposed design for implementation of 8 by 8 memory array.

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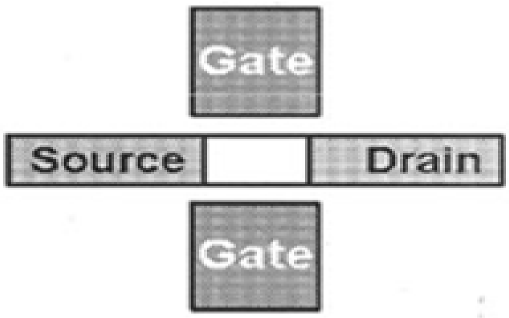

Figure 1 Double Gate MOSFET

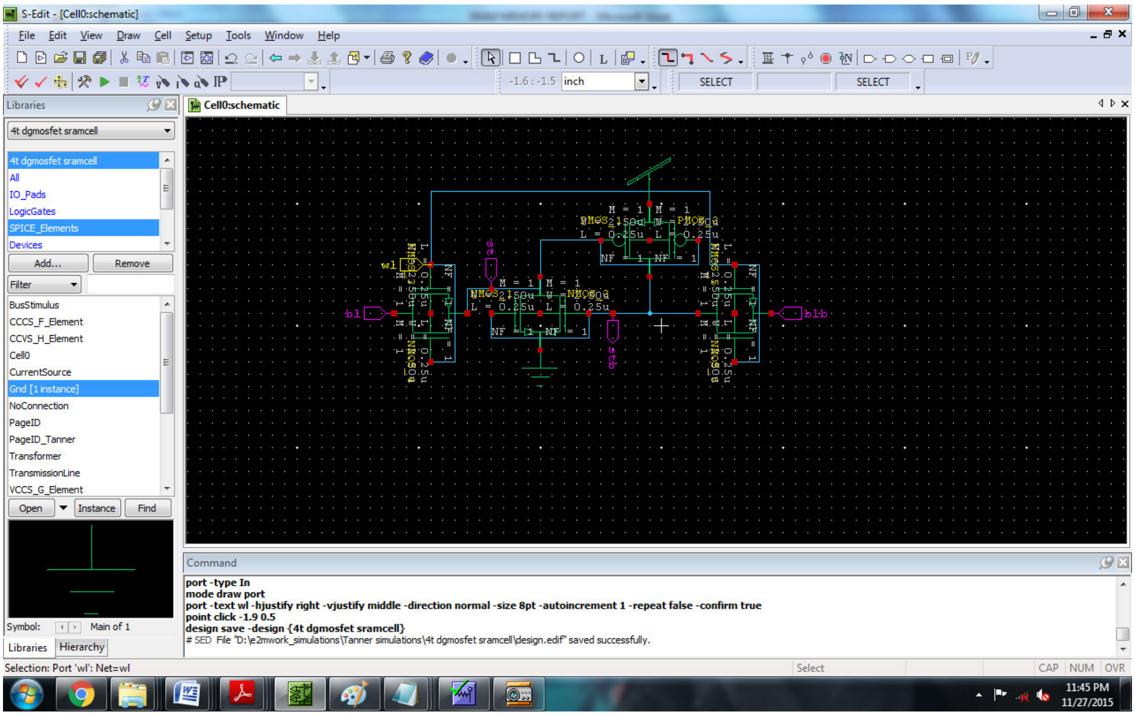

Figure 2 Proposed 4T SRAM

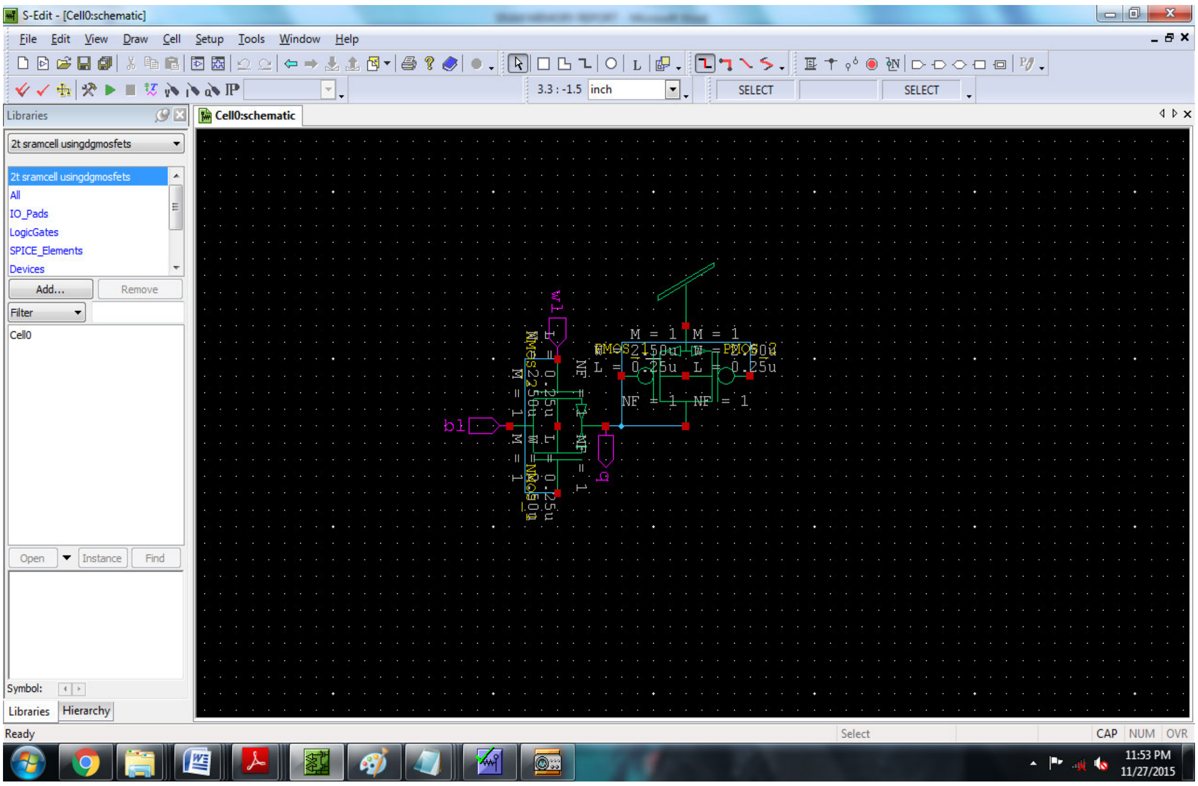

Figure 3 Proposed 2T SRAM

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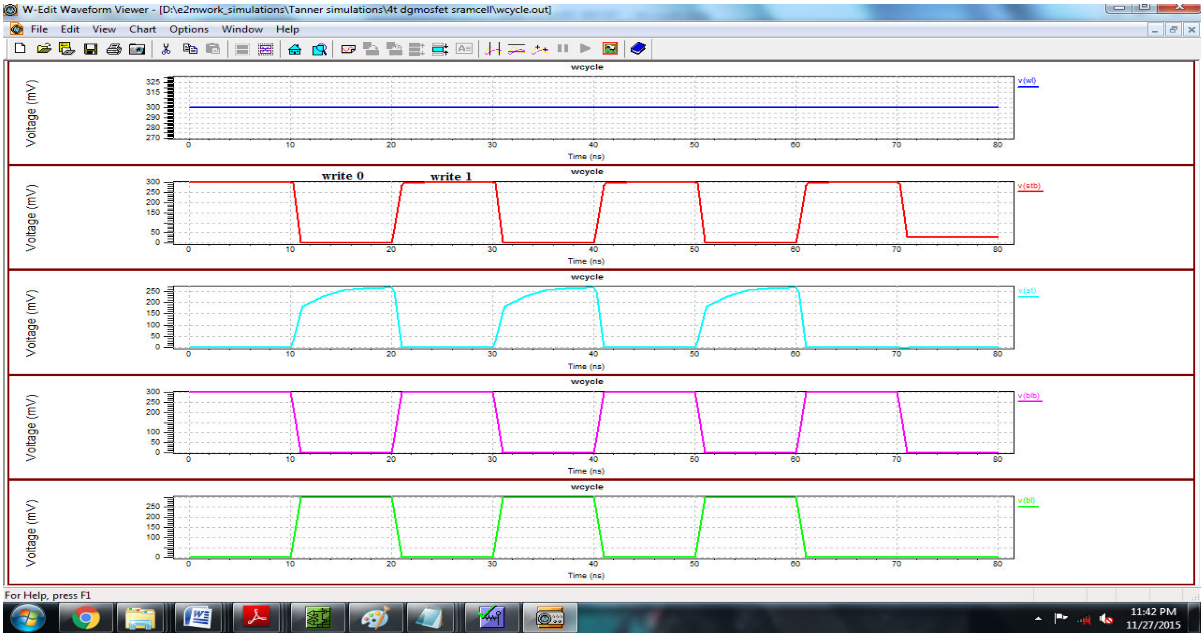

Figure 4 write cycle for Proposed 4T SRAM

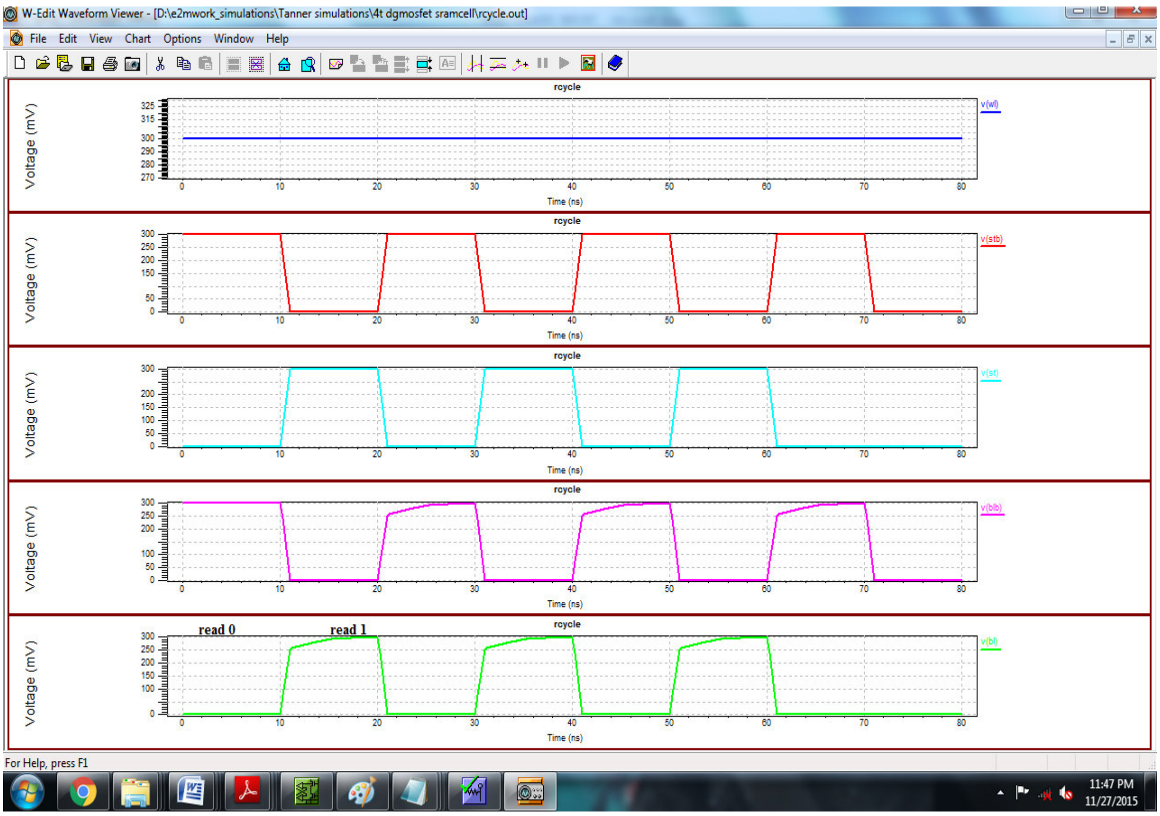

Figure 5 read cycle for Proposed 4T SRAM

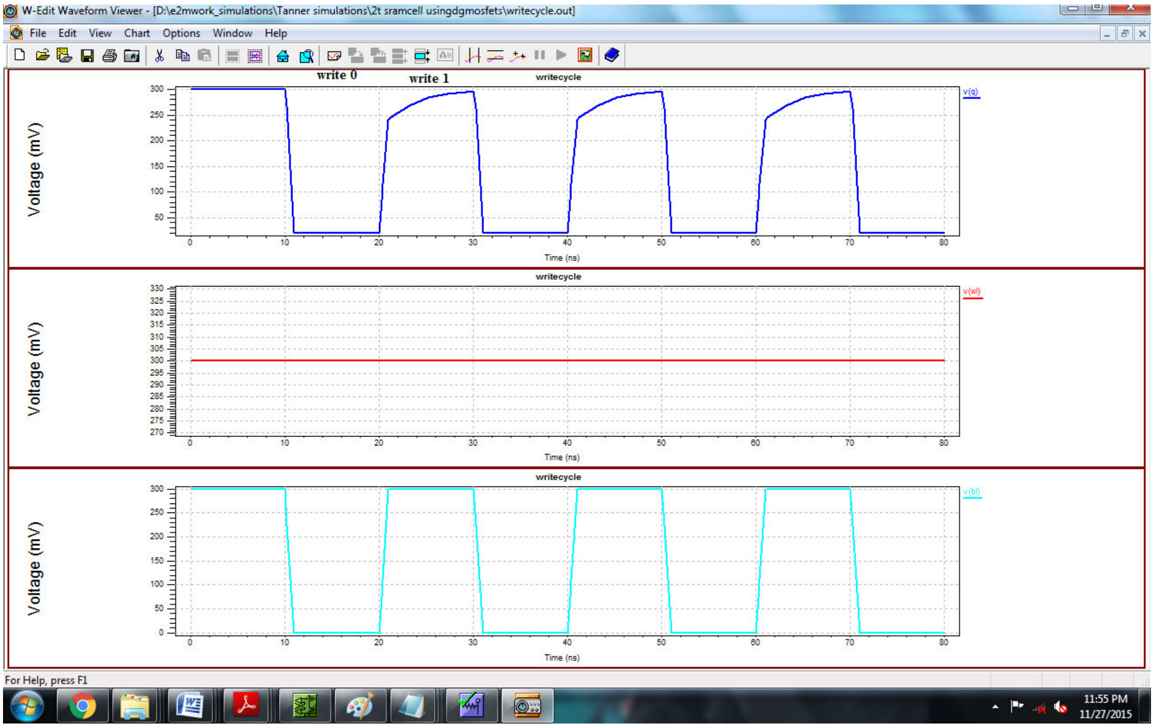

Figure 6 write cycle for Proposed 2T SRAM

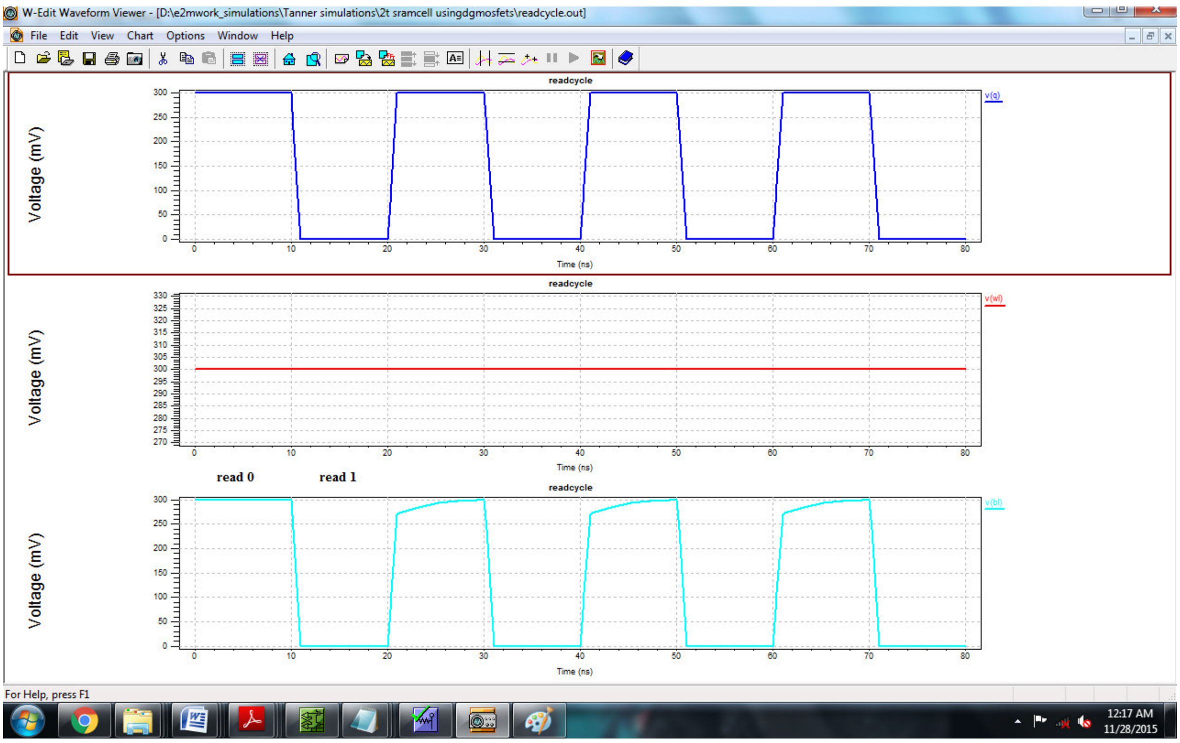

Figure 7 read cycle for Proposed 2T SRAM

Table 1   Comparison of different Parameters for proposed 4T and 2T cells

	Parameters	**Proposed 4T**	**Proposed 2T**
1	**Technology**	45nm	45nm
2	**Power dissipation for write cycle**	38.5 nw	110 nw
3	**Power dissipation for read cycle**	40 nw	154 nw
4	**PDP for write cycle**	361 e-18-watt-sec	1.254 e-15-watt-sec
5	**PDP for read cycle**	364 e-18-watt-sec	1.590 e-15-watt-sec