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Memristor-Based Resistive Random Access Memory: Hybrid Architecture for Low Power Compact Memory Design

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Abstract
The computer memory system has both volatile and non volatile memory. The Volatile memories such as SRAM and DRAM used as a main memory and non volatile memory like flash memory. But in recent days new non volatile technologies are invented that promise the rapid changes in the landscape of memory systems. Memristor is a two terminal passive element whose resistance depends on the magnitude and polarity of the voltage applied to it. It has nonlinear relationship between voltages and current which is similar to memory devices. In this paper we approach to design memristor based nonvolatile 6-T static random access memory (SRAM) and analysis the circuit performance with conventional 6-T SRAM cell in order to prove the parameter optimizations. Then we address the memristor-based resistive random access memory (MRRAM) which is similar to that of static random access memory (SRAM) cell and we compare the nonvolatile characteristics of MRRAM with SRAM cell.
Index terms: NV memory, memristor, SRAM, Resistive RAM, SPICE model.

1. Introduction

Leon Chua [1] envisioned the fourth non-linear passive two terminal electrical component called memristor in 1971. It relates electric charge and magnetic flux linkage for a particular time interval. In 2008, researchers at Hewlett Packard (HP) Labs reported that the memristor was realized physically using thin film of titanium dioxide nanoscale device [2]. Basically the memristor is a resistance with memory. Its resistance chances when a voltage is applied to this element and remains constant on that particular value when the applied voltage is removed. The main difference between the memristor (M) and the three passive elements (R, L, C) is its nonlinear input-output characteristics. Memristors are also used as programmable resistive loads in a differential amplifier [7]. Memristor act as a strong candidate for future memories because of its non-volatile property and high packing density in a crossbar array [11]. The main feature of our circuit is its non-volatility and its reduced size compared to the conventional 6T-SRAM. The data is retained in the memory even when the power is turned off for an indefinite time. The area can be much less than the conventional SRAM cells since each memory cell consists of only three transistors and two memristors.

Resistive RAM is a device that can switch between one or more resistances under the application of appropriate voltages. It shows memristive behavior, and can be thought of as a specific type of memristor. Devices can have two or more discrete resistance states, or may have a continuously variable resistance. Whatever the case, it is important that the change in resistance is governed by the past history of the device - that is, by the previous voltage applied, or the previous current that has flowed through the device. RRAM devices may help overcome some of the bottlenecks that we are currently facing in microelectronics.

The paper starts off with the introduction of memristor and its characteristics. After that some related works and the structure of the memristor based SRAM circuit, its working principle and the functionality. Then it discusses the perspectives, draws some comparisons and finally it concludes with the
prospects of memristive based resistive RAM circuit.

2. Memristor characterization

The memristor was defined in terms of a non-linear functional relationship between the magnetic flux $\Phi_m(t)$ and the amount of electric charge that has flowed through it q(t),

$$f(\Phi_m(t),q(t)) = 0$$

The variable Φ_m (“magnetic flux”) is generalized from the circuit characteristic of an inductor. It does not represent a magnetic field here. The symbol Φ_m may be regarded as the integral of voltage over time [20].

Each memristor is characterized by its memristance function describing the charge-dependent rate of change of flux with charge.

$$M(q) = \frac{d\Phi m}{dq}$$

Substituting the flux as the time integral of the voltage, and charge as the time integral of current, the more convenient form is

$$M(q(t)) = \frac{d\Phi m/dt}{dq/dt} = \frac{V(t)}{I(t)}$$

The relationship between memristor and other three elements are shown in the following figure. No device can relate dI to dq, or $d\Phi_m$ to dV, because I is the derivative of Q and Φ_m is the integral of V. It can be known from this that the memristance is charge-dependent resistance.

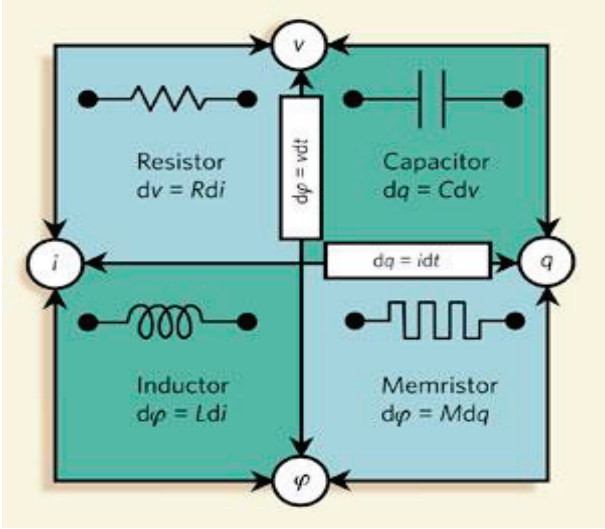


Figure 1. Relationship between three basic components and memristor

If M(q(t)) is a constant, then we obtain Ohm's Law R(t) = V(t)/ I(t). If M(q(t)) is a variance, however, the equation is not equivalent because q(t) and M(q(t)) can vary with time. Solving for voltage as a function of time produces the following equation,

$$V(t) = M(q(t))I(t)$$

This equation shows that memristance defines a linear relationship between current and voltage, as long as M does not vary with charge. Nonzero current implies time varying charge. Furthermore, the memristor is static if no current is applied. If I(t) = 0, we find V(t) = 0 and M(t) is constant. This is the fundamental nature of the memory effect.

$$P(t) = I(t)V(t) = I^2(t)M(q(t))$$

As long as M(q(t)) varies slightly, such as under alternating current, the memristor will appear as a constant resistor. If M(q(t)) increases rapidly, however, current and power consumption will speedily stop. M(q) is physically restricted to be positive for all values of q (assuming the device is passive and does not become superconductive at some q). A negative value would mean that it would continuously supply energy when operated with alternating current. For $R_{ON} << R_{OFF}$ the memristance function was determined to be

$$M\,q(t)) = R_{OFF} \cdot \left(1 - \frac{\mu_v R_{ON}}{D^2} q(t)\right)$$

Where R_{OFF} represents the high resistance state, R_{ON} represents the low resistance state, μ_v represents the mobility of dopants in the thin film, and D represents the film thickness.

3. Memristor as a switch

For some memristors, applied current or voltage causes significant change in resistance value. Such devices may be characterized as switches by investigating the time and energy that must be spent to achieve a desired change in resistance. This assumes that the applied voltage remains constant. Solving for energy dissipation during a single switching event shows that for a memristor to switch from R_{on} to R_{off} in time T_{on} to T_{off}, the charge must change by $\Delta Q = Q_{on} - Q_{off}$. The final expression can be derived as,

$$E_{switch} = V^2 \int_{T_{off}}^{T_{on}} \frac{dt}{M(q(t))} = v^2 \int_{Q_{off}}^{Q_{on}} \frac{dq}{I(q)M(q)} = V^2 \int_{Q_{off}}^{Q_{on}} \frac{dq}{V(q)} = V\Delta Q$$

Substituting V=I(q)M(q), and then $\int dq/V = \Delta Q/V$ for constant VTo produces the final expression. This power characteristic differs primarily from that of a metal oxide semiconductor transistor, which is capacitor-based. Unlike the transistor, the final state of the memristor in terms of charge does not depend on bias voltage.The type of memristor described by Williams ceases to be ideal after switching over its entire resistance range, creating hysteresis, also called the "hard-switching regime" [14]. Another kind of switch would have a cyclic M(q) so that each off-on event would be followed by an on-off event under constant bias. Such a device would act as a memristor under all conditions, but would be less practical.

4. Working principle of memristor

Srrukov et al. [2] introduced a physical model of the memristor. They have shown that the memristor can be characterized by an equivalent time-dependent resistor whose value at a time t is linearly proportional the quantity of charge q that has passed through it. The HP device memristor is composed of a 50nm thin film of titanium dioxide sandwiched between two 5 nm thick electrodes. Initially, there are two layers to the titanium dioxide film, one of which has a slight depletion of oxygen atoms. The oxygen vacancies act as charge carriers, meaning that the depleted layer has a much lower resistance than the non-depleted layer. When an electric field is applied, the oxygen vacancies drift, changing the boundary between the high-resistance and low-resistance layers. Thus the resistance of the film as a whole is dependent on how much charge has been passed through it in a particular direction, which is reversible by changing the direction of current [14]. Since the HP device displays fast ion conduction at nanoscale, it is considered as a nanoionic device [5].

The resistance change is non-volatile hence the cell acts as a memory element. Fig. 2(a) shows the doped and undoped region of a memristor. If a voltage is applied across the memristor,

$$v(t) = M(t)i(t)$$

$$M(t) = R_{ON}\frac{w(t)}{D} + R_{OFF}\left(1 - \frac{w(t)}{D}\right)$$

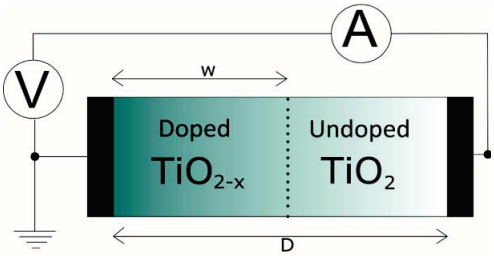
Where R_{ON} is the resistance of completely doped memristor and R_{OFF} is the resistance of completely undoped memristor.

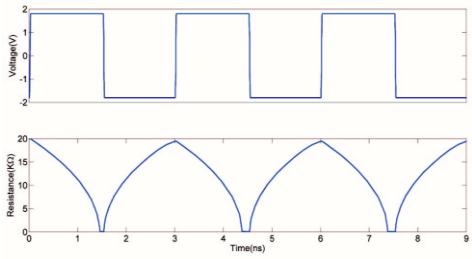
Then w(t) is given by

$$\frac{dw(t)}{dt} = \mu_v \frac{R_{ON}}{D} i(t)$$

μ_v is the average dopant mobility and D is the length of the memristor. From these equations, the considered nonlinearity produced from the edge of the thin film can be obtained as

$$f(\frac{w(t)}{D}) = 1-(2\frac{w(t)}{D} - 1)^{2p}$$





(a) (b)

Figure 2. (a) Characterizing the memristor and (b) Change of resistance when a 3.6V p-p square wave is applied. Resistance of the memristor changes from 20KΩ to 100Ω in positive cycle and this change occurs in reverse direction when the square pulse reverses its direction.

5. Related works

Static random-access memory (SRAM) is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The term static differentiates it from dynamic RAM (DRAM) which must be periodically refreshed. SRAM exhibits data remanence [1], but it is still volatile in the conventional sense that data is finally lost when the memory is not powered. The operation of SRAM cell has three different states. It can be in: standby (the circuit is idle), reading (the data has been requested) and writing (updating the contents). The SRAM to operate in read mode and write mode should have "readability" and "write stability" respectively.

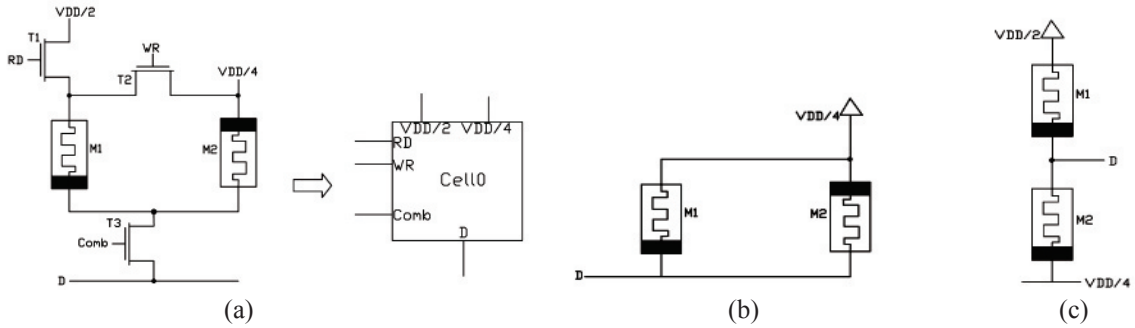
The most commonly used SRAM type is the 6T SRAM which offers better electrical performances from all aspects (speed, noise immunity, standby current). The smallest 6T-SRAM cell that has been fabricated till today has an area of $0.08\mu m^2$ and it was fabricated in the 22 nm process using immersion and EUV lithography [15]. The main disadvantages of the 6T SRAM structure are its large size and high power consumption. To overcome these limitations, memristive-RAMs are being developed recently. According to HP, resistive random access memory (ReRAMs), which are memristor-based versions of both DRAM and SRAM, ought to speed up computers immensely. In [16], a complementary resistive switch was introduced which consisted of two anti-serial memristive elements which validates the construction of large crossbar arrays with a reduced power consumption.

6. Memristor based SRAM

Electrical scheme of the proposed SRAM cell is shown in Fig. 3(a). Two memristors are acted as memory element. The arrangement is in such a way that during write cycle, they are connected in parallel but in opposite polarity [Fig. 2(b)] and during read cycle, they are connected in series [Fig. 2(c)].These connections are recognized by two NMOS pass transistors T1 and T2. A third transistor T3 is used to isolate a cell from other cells of the memory array during read and write operations. The gate input of T3 is the Comb signal which is the OR of RD (Read) and WR (Write) signals. RD is set to the LOW state and WR and Comb are set to the HIGH state for write operation. As a result, circuit of Fig. 3(b) is formed. The voltage across the memristors here is (*VD*-*VDD*/4). Depending on the data, it can be either positive (*VD*= *VDD*) or negative (*VD*= 0 V). Since the polarities of the memristors are opposite, change of memristances (or resistances) will also occur in the opposite direction. Now RD and Comb are kept in the HIGH state and this forms the circuit shown in Fig. 3(c).
Voltage at *D* is now:

$$V_D = \left(\frac{V_{DD}}{2} - \frac{V_{DD}}{4}\right) \times \frac{R2}{(R1+R2)} + \frac{V_{DD}}{4}$$

Where, R1 and R2 are the resistances of M1 and M2 respectively. If "1" was written during write cycle, R2 becomes significantly greater than R1 (R2<R1) and then VD is greater than VDD/4 (VD<VDD/4). If "0" was written, *R*1 becomes significantly greater than *R*2 (R1<R2) which makes *VD* to be as close as *VDD*/4. A comparator can be used as a sense amplifier to translate these voltages as HIGH or LOW properly.



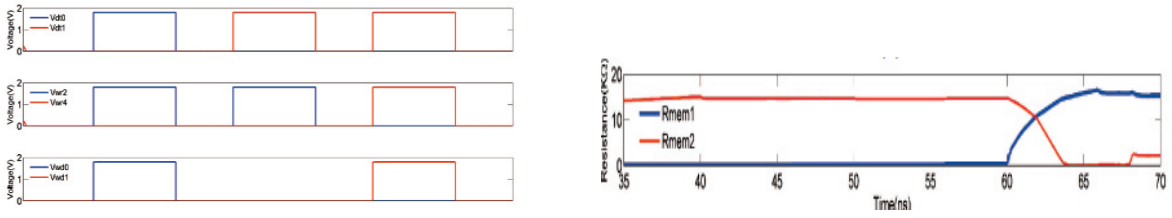
(a) (b) (c)

Figure 3. (a) Three transistor-two memristor SRAM cell (b) Circuit when rd=0, wr=1, and comb =1. (c) Circuit when rd=1, wr=0, and Comb=1.

7. Simulations

A 16 x 16 array is considered for the verification of array structure of the NVRAM cell. Data is given through word lines/bit lines and switching is controlled by the Vdt and Vdtb signals. In the simulations data was written and read to calculate a number of important factors such as write time, read time, power consumption etc. A comparator is used as a sense amplifier to translate these voltages as perfect '1' and '0' and the reference of this should be fixed to 0.26V. Simulation results are based on the following parameters: R_{ON} = 100Ω, R_{OFF} = 20kΩ, p=10, D=3nm and $\mu_v = 350 \times 10^{-9}$ $m^2/s/V$.

7.1. Write operation



(a) (b)

Figure 4. (a) Timing diagram of input pulses during write operation. (b) Change of resistance of the two memristors of cell20 during write operation.

In cell2, "1" was written during the first write cycle. Vwr2, Vrow0 and Vdt0 were set to HIGH state to select this cell. Timing diagram in Fig. 4(a) shows Vwr2, Vdt0 pulses and also shows the data in d0 which is Vwd0. This write cycle starts from 40 ns and during this cycle, Vwr2=1, Vdt0=1 and Vwd0=1. In the next cycle, a "0" was written to cell18 (from 50 ns) and to do this, Vwr2, Vrow1, Vdt1 were set to HIGH state and Vwd1 was set to LOW state. Finally a "1" was written to cell20 (from 60 ns). For this, Vwr4, Vrow1,Vdt1 and Vwd1, all were set to HIGH state. In Fig. 4(b), plot of the resistance of two memristors in cell20 shows the alteration of resistance while writing "1" into it.

7.2. Read operation

After the write operation in cell 2, the stored data was read from 48 ns. For this, Vrd2 was set to HIGH state and data at dn0 is assured. Timing diagram of read cycles is shown in figure 5. After writing "1" in cell 18, all the power sources are turned off during the time interval 50-69 ns. A read operation is done after turning on the power sources and found "1" in cell 18. During read operation at cell2, dn0 was established HIGH. Then after two write cycles, cell20 was read from 68 ns and found HIGH at dn1. At last, cell18 was read from 69 ns and originated LOW at dn1. So after reading a cell, data was found to be exactly the same as it was written previously in that cell. Hence, the array structures illustrate proper functionality both in read and write operations.

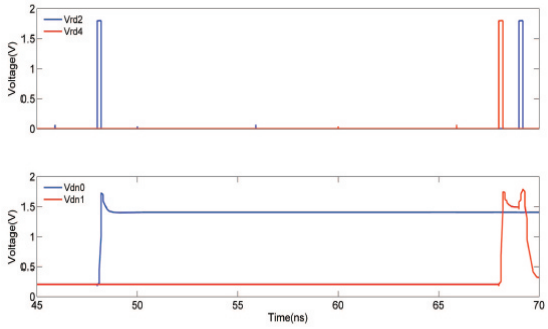


Figure 5. Proof of non-volatility of the memristor SRAM cell.

7. Perspectives

The memristor based memory cell exhibits non-volatile property in nature. After writing "1" in cell 18, all the power sources were turned off during the time interval 50-69 ns (Fig. 5). A read operation is carried out after turning on the power sources and detected "1" in cell 18. This demonstrates the non-volatile property of the cell. The write time and read time were calculated and compared in Table 1. The NVRAM cell needs a bit more time for the write cycle than the conventional SRAM cells. This can be overcome by further increasing the mobility of the memristors. From the simulation result, the integration was made to get the dissipated energy for separate operations (write "1" & "0" and read "1" & "0").

Table 1. Write/read time comparison.

Operation	Proposed SRAM cell(ns)	6-T cell(ns)
Write operation	5.87	0.90
Read operation	0.19	1.36

Then the energy values were divided by respective operation cycle times to get the corresponding power dissipations (Table 2). Then the determined values were averaged to get the total power dissipation. This was compared with the value of the conventional SRAM cell in Table 3. This shows that the power consumption is much less than 6-T and the area of the NVRAM cell can be found to be much less since only three transistors are used along with two memristors as memory element.

Table 2. Power dissipation of Read /Write operation

Operation	Wr0	Wr1	Rd0	Rd1
Energy (fJ/ cycle)	190.8	803.5	61.4	67.9
Power (μW)	32.4	136.2	306.6	339
Peak power (mW)	0.94	2.6	5.81	5.92

Table 3. Power comparison

Operation	Proposed SRAM cell(mW)	6-T cell (mW)
Power	0.410	10.380

8.Conclusion

In this paper, we intended a new idea of NVRAM cell using memristor. The read time is much faster compared to a conventional SRAM and the power consumption is also much smaller. However the writing speed is not satisfactory compared to existing SRAM cells due to the low mobility of the memristor in the SPICE model we used. Recent researches suggest that the write time can be significantly reduced [14], [20] using state-of-the-art fabrication techniques and also by using memristor based RRAM. There are further scopes to work on power consumption as well. Overall, it can be said that our proposed memristor based RRAM is a combination of new technology and innovative design which can open a new door in the field of memory design.

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