Control Theory and Informatics
ISSN 2224-5774 (print) ISSN 2225-0492 (online)
Vol.3, No.2, 2013- National Conference on Emerging Trends in Electrical, Instrumentation & Communication Engineering

Control of DSTATCOM in 3-Phase 3-Wire Distribution System using Modified *IcosØ* Algorithm

Bhim Singh[1] , Sunil Kumar [2]
[1] Department of Electrical Engineering, Indian Institute of Technology, New Delhi
[2]Aerial Delivery Research & Development Establishment, Agra
[1] Email- bhimsinghr@gmail.com
[2] mr.sunil.kr@gmail.com

Abstract-
In this paper, a 3-leg VSC (voltage source converter) based DSTATCOM (Distribution Static Compensator) is used for load compensation in 3-phase 3-wire distribution system. The control algorithm is based on *IcosØ* algorithm. This modified IcosØ algorithm is used for extracting the reference source currents for Power Factor Correction, Load Balancing and Voltage Regulation at PCC (point of common coupling). For various load conditions such as a reactive linear load, an unbalanced load and a non-linear load, Simulations are performed for Power Factor Correction (PFC) mode and Zero Voltage Regulation (ZVR) mode in MATLAB environment using SIMULINK and SimPowerSystem toolbox. Steady state and dynamic results on a developed hardware prototype of DSTATCOM are also presented to validate the control algorithm for DSTATCOM.
Keywords-DSTATCOM, Control algorithm, Power quality, Nonlinear load, Load balancing, Harmonics compensation, Voltage regulation.

1. Introduction

In present time, distribution system is facing the poor power quality problems such as poor power factor, unbalanced loading of three phases, voltage drop and harmonic injection. The reasons for the poor power quality are reactive, unbalanced and nonlinear loads (such as motors, adjustable speed drives (ASDs), variable frequency drives (VFDs) and power electronic converter) used in domestic and industrial applications. The reactive loads affect the active power flow and cause the voltage drop at load end point. Moreover, the nonlinear loads (ASDs, VFDs and power electronic converter) inject the harmonics in the system which distorts the voltages at PCC and affect the performance of other loads connected to same terminals. Such power quality problems can be mitigated by connecting the DSTATCOM at PCC [1-5].
For compensating the reactive load, load balancing and harmonic elimination in three phase distribution system, a number of topologies of DSTATCOM are reported in the literature such as a 3-leg VSC [3] and H-bridge VSC with split capacitor [6-7]. For extracting the reference source currents to control the DSTATCOM, many control algorithms such as Instantaneous Reactive Power (IRP) theory, Synchronous Reference Frame (SRF) theory, PI controller based algorithm and Adaline neural network based algorithm [6] are reported in the literature [1-5].

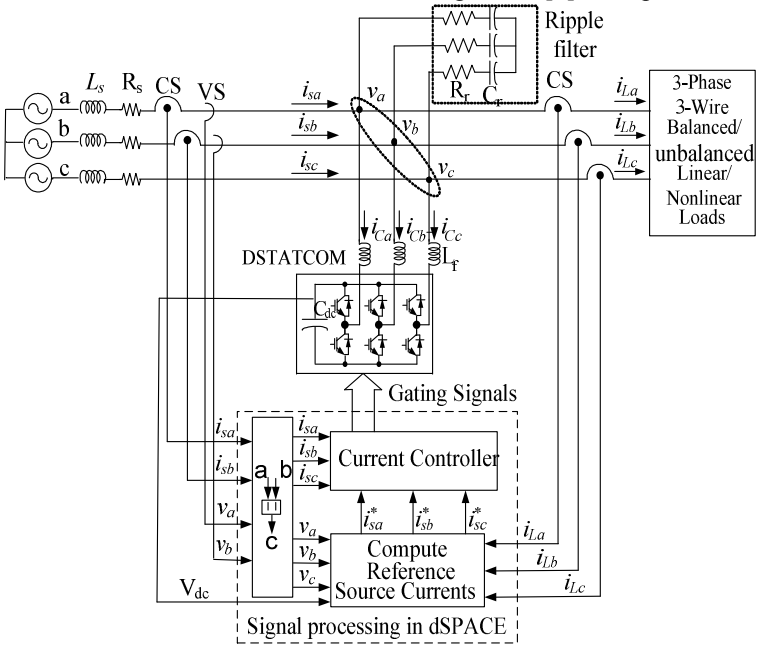


Figure 1. Block diagram of power and control circuit of DSTATCOM.

Initially *IcosΦ* algorithm is proposed for the active filter for power factor correction [10-12]. In this paper, modified *IcosΦ* algorithm [13] is used for Power Factor Correction, Load Balancing and Voltage Regulation at PCC in three phase three wire distribution system. The advantage of modified *IcosΦ* algorithm is that it is capable to detect the load variation within one sixth cyclic time of source frequency and gives the fast response and has capability of voltage regulation. The modified control algorithm is used with indirect current control scheme for controlling the current of the DSTATCOM as the source currents are slow varying currents. The extracted reference source currents (i_{sa}^*, i_{sb}^* and i_{sc}^*) are compared with the respective sensed source currents (i_{sa}, i_{sb} and i_{sc}) and current errors are used to generate the switching pattern for controlling the DSTATCOM. A DSTATCOM is implemented with modified *IcosΦ* algorithm in PFC mode and ZVR mode in MATLAB environment using SIMULINK and SimPowerSystem toolboxes. A dSPACE- digital signal processor is used for hardware implementation. The performance of DSTATCOM is studied to compensate the load harmonics currents and load balancing in PFC mode and ZVR mode in 3-phase 3-wire distribution system.

2. SYSTEM CONFIGURATION

The basic circuit diagram of a 3 leg VSC based DSTATCOM with signal sensing is shown in Fig. 1. The DSTATCOM consists of a 3-leg VSC is connected to the three phase three wire distribution system in parallel to a three phase loads. Three phase loads may be a reactive load or an unbalance load or a non linear load and a combination. A three-phase VSC is realized using six IGBTs (insulated gate bipolar transistors) switches with anti parallel diodes. Three phase VSC is connected through interfacing inductors at AC side for reducing ripples in compensating currents. For reducing switching ripples of DSTATCOM in the PCC voltage, a RC filter is connected to the system in parallel to DSTATCOM. The DSTATCOM is controlled with modified *IcosΦ* algorithm for the compensation of reactive and harmonic currents of the load and unbalanced load for correcting the power factor at source side or regulating the voltage at PCC. DSTATCOM injects the currents to maintain the unity power factor on source side or to regulate the PCC voltage at the desired reference value of the voltage by injecting the required reactive power. In PFC mode, there is no phase difference between the PCC voltage and source currents. In ZVR mode, the source currents may be leading or lagging currents depending on the reference PCC voltage and load on the system.

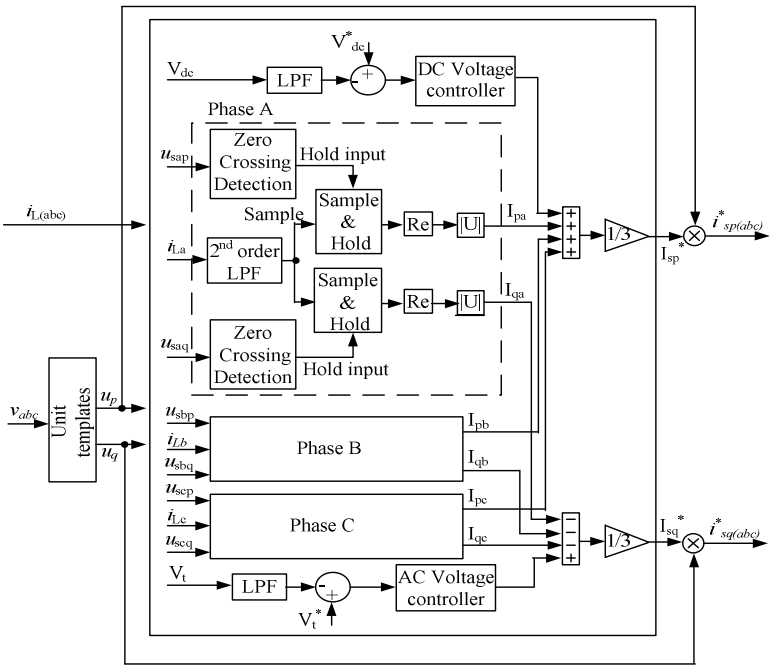


Figure 2. Block diagram of extracting reference source currents using modified IcosΦ algorithm based Controller.

3. CONTROL ALGORITHM

The modified *IcosΦ* control algorithm based on *IcosΦ* algorithm [10-12] is shown in Fig. 2. The PCC voltage (v_a, v_b and v_c), the source currents (i_{sa}, i_{sb} and i_{sc}), the load currents (i_{La}, i_{Lb} and i_{Lc}) and the DC bus voltage (V_{dc}) of the DSTATCOM are sensed as feedback signals for extracting the reference source currents. In control algorithm, it is considered that the source supplies only the active component of the load currents i.e. *IcosΦ* component of the load current (where I=amplitude of fundamental load current, Φ= displacement angle of load current w.r.t. PCC voltage). In modified control algorithm, the reference source currents are generated by the sum of product

of *IcosΦ* and *IsinΦ* component of load currents with unit templates. For an instant three phase load current can be expressed as:

$$i_{La}=\sum_{n=1}^{\infty}I_{Lan}\sin\left(n\omega t-\phi_{an}\right);\ i_{Lb}=\sum_{n=1}^{\infty}I_{Lbn}\sin\left(n\omega t-\phi_{bn}-120°\right);\ i_{Lc}=\sum_{n=1}^{\infty}I_{Lcn}\sin\left(n\omega t-\phi_{cn}-240°\right) \quad (1)$$

where $ø_{(abc)1}$ and $ø_{(abc)n}$ are phase angles of fundamental and nth harmonic current in a, b, and c phases. $I_{L(abc)1}$ and $I_{L(abc)n}$ are amplitude of fundamental and nth harmonic current in a, b, and c phases.

The magnitudes of active component of fundamental load currents are given as:

$$\left|\mathrm{Re}(I_{La1})\right|=\left|I_{La1}\right|\cos\phi_{a1};\ \left|\mathrm{Re}(I_{Lb1})\right|=\left|I_{Lb1}\right|\cos\phi_{b1};\ \left|\mathrm{Re}(I_{Lc1})\right|=\left|I_{Lc1}\right|\cos\phi_{c1} \quad (2)$$

At the zero crossing of the unit template (in phase of PCC voltage), the amplitude of active component of fundamental load current (*IcosΦ*) is extracted from the load currents by shifting the load currents by +90°, using a set of low pass filters. The filters are used with 50Hz cut-off frequency to extract the fundamental load current so that no harmonic is presented in sensed load current. A zero crossing detector is used to detect the zero crossing instant of in-phase unit template and a "sample and hold" circuit is used to take the sample of load current at that zero crossing instant of corresponding in-phase unit template that gives *IcosΦ* component of the load current (active current of the load current). The magnitude of active component of reference source currents for balanced source currents can be expressed as:

$$I_{sp}^{*}=\left(\left|I_{La1}\right|\cos\phi_{a1}+\left|I_{Lb1}\right|\cos\phi_{b1}+\left|I_{Lc1}\right|\cos\phi_{c1}+I_{d}\right)/3 \quad (3)$$

where $|I_{La1}|\cos\Phi_{a1}$, $|I_{Lb1}|\cos\Phi_{b1}$ and $|I_{Lc1}|\cos\Phi_{c1}$ are the amplitude of the load active currents and I_d is the output of the PI controller over the DC bus voltage for the self supporting bus of the DSTATCOM which can be expressed as:

$$I_{d}=K_{pd}V_{dce}+K_{id}\int V_{dce}dt \quad (4)$$

where $V_{dce}=V_{dc}^{*}-V_{dc}$ = error in DC bus voltage of DSTATCOM. V_{dc}^{*}= reference DC bus voltage of DSTATCOM and V_{dc}=sensed DC bus voltage of DSTATCOM respectively. K_{pd} and K_{id} are the proportional and integral gains of the PI controller over the DC bus voltage of DSTATCOM given in eqn. (4).

Active component of three phase source currents can be obtained with in-phase unit templates as:

$$i_{sap}^{*}=I_{sp}^{*}\ u_{sap};\quad i_{sbp}^{*}=I_{sp}^{*}\ u_{sbp};\quad i_{scp}^{*}=I_{sp}^{*}\ u_{scp}; \quad (5)$$

Similarly from the filtered fundamental load currents, the amplitude of reactive component (*IsinΦ*) of fundamental load currents can be extracted at the zero crossing of the unit template in quadrature of PCC voltage. The magnitude of reactive component of the reference source currents can be expressed as:

$$I_{sq}^{*}=\left\{-\left(\left|I_{La1}\right|\sin\phi_{a1}+\left|I_{Lb1}\right|\sin\phi_{b1}+\left|I_{Lc1}\right|\sin\phi_{c1}\right)+I_{a}\right\}/3 \quad (6)$$

where $|I_{La1}|\sin\Phi_{a1}$, $|I_{Lb1}|\sin\Phi_{b1}$ and $|I_{Lc1}|\sin\Phi_{c1}$ are the amplitude of reactive load currents. The negative sign with the *IsinΦ* terms is used because there is a phase difference of 180° between quadrature template of the PCC voltage and the filtered fundamental reactive load current. I_a is the output of the AC bus voltage controller to regulate the voltage at PCC that can be expressed as:

$$I_{a}=K_{pa}V_{e}+K_{ia}\int V_{e}dt \quad (7)$$

where $V_e=V_t^{*}-V_t$ = error in amplitude of the PCC voltage. V_t^{*}= reference amplitude of PCC voltage and V_t sensed amplitude of PCC voltage. K_{pa} and K_{ia} are the proportional and integral gains of the PI controller over the PCC voltage given in eqn. (7).

Three phase reactive component of reference source currents can be obtained with quadrature unit templates as:

$$i_{saq}^{*}=I_{sq}^{*}\ u_{saq};\quad i_{sbq}^{*}=I_{sq}^{*}\ u_{sbq};\quad i_{scq}^{*}=I_{sq}^{*}\ u_{scq}; \quad (8)$$

The total three phase reference source currents can be obtained from eqn. (5) and eqn. (8) as:

$$i_{sa}^{*}=i_{sap}^{*}+i_{saq}^{*};\quad i_{sb}^{*}=i_{sbp}^{*}+i_{sbq}^{*};\quad i_{sc}^{*}=i_{scp}^{*}+i_{scq}^{*}; \quad (9)$$

These reference source currents (i_{sa}^{*}, i_{sb}^{*} and i_{sc}^{*}) are compared with the respective sensed source currents (i_{sa}, i_{sb} and i_{sc}) and resultant current errors after the amplification are used to generate the switching signals for controlling of the DSTATCOM. For power factor correction, I_{sq}^{*} is kept zero as no reactive current is supplied by the source.

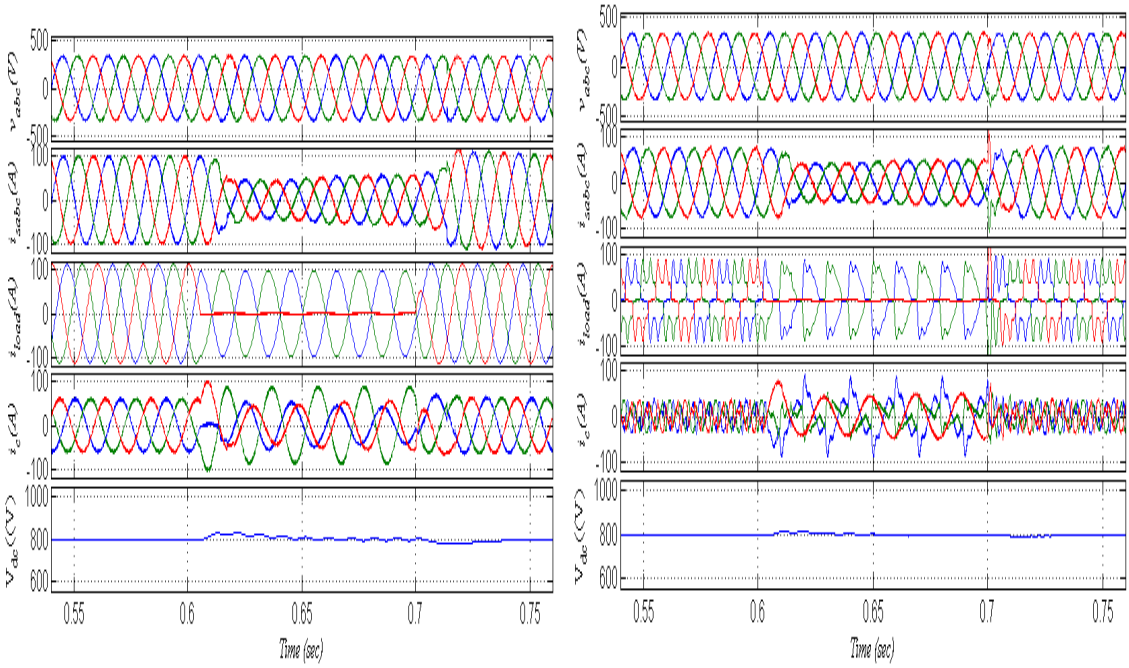
4. SIMULATION RESULTS AND DISCUSSION

The performance of DSTATCOM in three phase three wire distribution system is studied with the modified IcosØ algorithm. The parameters of DSTATCOM are given in Appendix-A. Initially considered linear reactive load is 46 kW, 0.8 lagging and nonlinear load is a three phase rectifier with a DC resistive load of 9Ω and a capacitor of 220µF in parallel. The PCC voltage is considered 415 V (L-L), which has nearly 340 V per phase (amplitude). The simulation results are taken for both PFC mode and ZVR mode for the same conditions.

Table 1 show the peak signal to noise ratio of performance of our proposed method of watermarked image and original image with various watermark image, where our watermarked images peak signal to noise ratio has a better performance than others. *4.1 Performance of DSTATCOM in PFC mode*

4.1.1With linear reactive load

The performance of DSTATCOM in PFC mode for load compensation (reactive and load balancing) is shown in Fig. 3. At t=0.6sec, three phase linear load is changed to two phase load and reapplied at t=0.7sec. The PCC voltages (v_{abc}), source currents (i_{sabc}), load currents (i_{Load}), compensator currents (i_c), and DC bus voltage (V_{dc}) are shown in Fig. 3(a). It is observed that these source currents are balanced and power factor is unity at source side irrespective of the balanced/unbalanced load conditions as the loads are compensated by the DSTATCOM. The DC bus voltage of DSTATCOM is also maintained to its reference value 800VDC.



(a) (b)

Fig. 3. Performance of DSTATCOM in PFC mode controlled by modified IcosΦ algorithm (a)with linear reactive load (b)with nonlinear load.

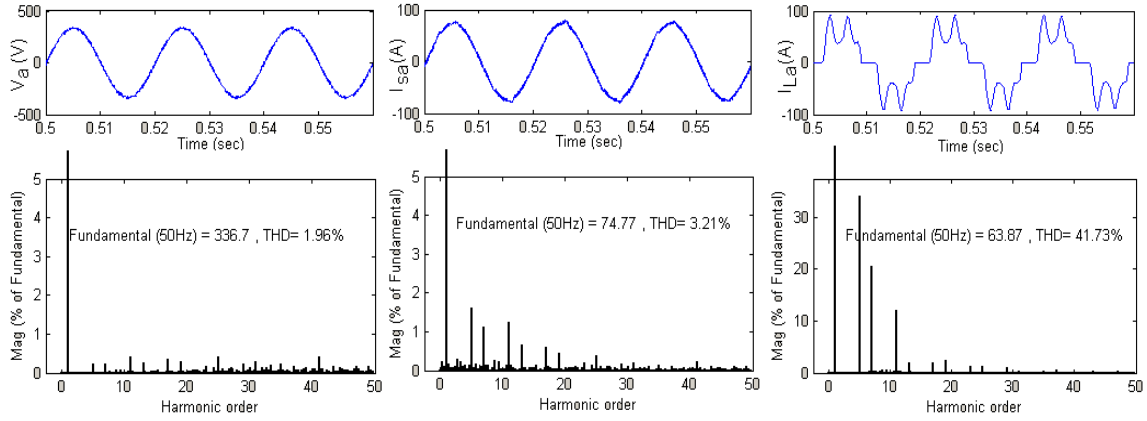
4.1.2With nonlinear load

In Fig. 3(b), the performance of the DSTATCOM for a nonlinear load in various loading conditions is shown. The nonlinear load is changed to two phase load and reapplied as in the case of linear load. Irrespective of balanced/unbalanced nonlinear loads, the source currents are found balanced, harmonic free and in phase of the PCC voltages. The DC bus voltage of DSTATCOM is also regulated to its reference value. The waveform and harmonic spectra of source voltage, source current and load current for phase A are shown in Figs. 4. The THD of source voltage and source current is found 1.96% and 3.21 % respectively when the THD of load current is 41.73% as shown in Figs. 4.

4.2 Performance of DSTATCOM in ZVR mode

4.2.1 with linear reactive load

The performance of DSTATCOM in ZVR mode with modified IcosØ algorithm is shown in Fig. 5(a). The load conditions are same as in PFC mode. It is observed that the PCC voltage is regulated to its reference amplitude of the PCC voltage (V_t^*=340V) and the source currents are balanced even when the loads are unbalanced. As the required reactive power to regulate the PCC voltage is injected by the DSTATCOM and load is compensated by the DSTATCOM.



(a) (b) (c)

Figs. 4. Waveform and THD spectrum of (a)PCC voltage of phase A (b)source current of phase A (c)load

4.2.1 with nonlinear load

The performance of DSTATCOM in ZVR mode for a nonlinear load is shown in Fig. 5(b). The nonlinear loads are compensated by the DSTATCOM to shape the source currents harmonic free and balanced during balanced/unbalanced nonlinear loads. The controller regulates the PCC voltage and DC bus voltage of DSTATCOM to their reference voltage. The waveform and harmonic spectra of source voltage, source current and load current is shown in Figs. 6. The source voltage THD is 2.27% and the THD of source current is found 5.01% when the THD of load current is 43.06% as shown in Figs. 6.

5. EXPERIMAENTAL VELIDATION

A laboratory prototype of DSTATCOM is developed using a 'Semikron' make 3-leg VSC consisting of six IGBTs and DC bus capacitor of 1650µF. The DSTATCOM system is connected to the 110V, 50Hz three phase supply system to study the performance for the various load conditions in the PFC mode. For controlling the DSTATCOM, five Hall effect current sensors (CS) (ABB EL50 P1 BB) and three Hall effect voltage sensors (VS) (ABB EM010 BBFHPIN) are used to get feedback signals such as PCC voltages, DC bus voltage, source currents and load currents as shown in Fig. 1. The modified IcosØ algorithm is implemented using the dSPACE digital signal processor. For recording the tests results, a Fluke 43B power analyzer and a four channels Digital Storage Oscilloscope of Agilent Technologies make are used. The DC bus voltage of DSTATCOM is regulated at 200V during these tests. The prototype of DSTATCOM is tested for three different load conditions in steady state as well as in dynamic conditions as discussed below.

5.1 performance of the dstatcom at balanced 0.8 lagging pf linear load

Figs. 7(a) and (b) show the source power and load power for a 0.8 pf lagging three phase load respectively. The power factor on source side is improved to unity while the power factor on load side was 0.8 lagging. In Figs. 7(c) and (d), the magnitude of source currents and load currents are shown with the line voltage of source. THD spectra of PCC voltages and source currents are shown in Figs. 7(e) & (f) respectively. The THD of source voltage and source current is found 1.7% and 2.5% respectively.

The phase voltage V_a, source current I_{sa}, load current I_{La}, and compensator current I_{Ca} of phase A are shown in Fig. 7(g).There is a phase difference between phase voltage and load current of phase A but there is no phase difference between the source voltage and source current as the reactive power of load is compensated by the DSTATCOM.

5.2 performance of the dstatcom with an unbalanced linear load

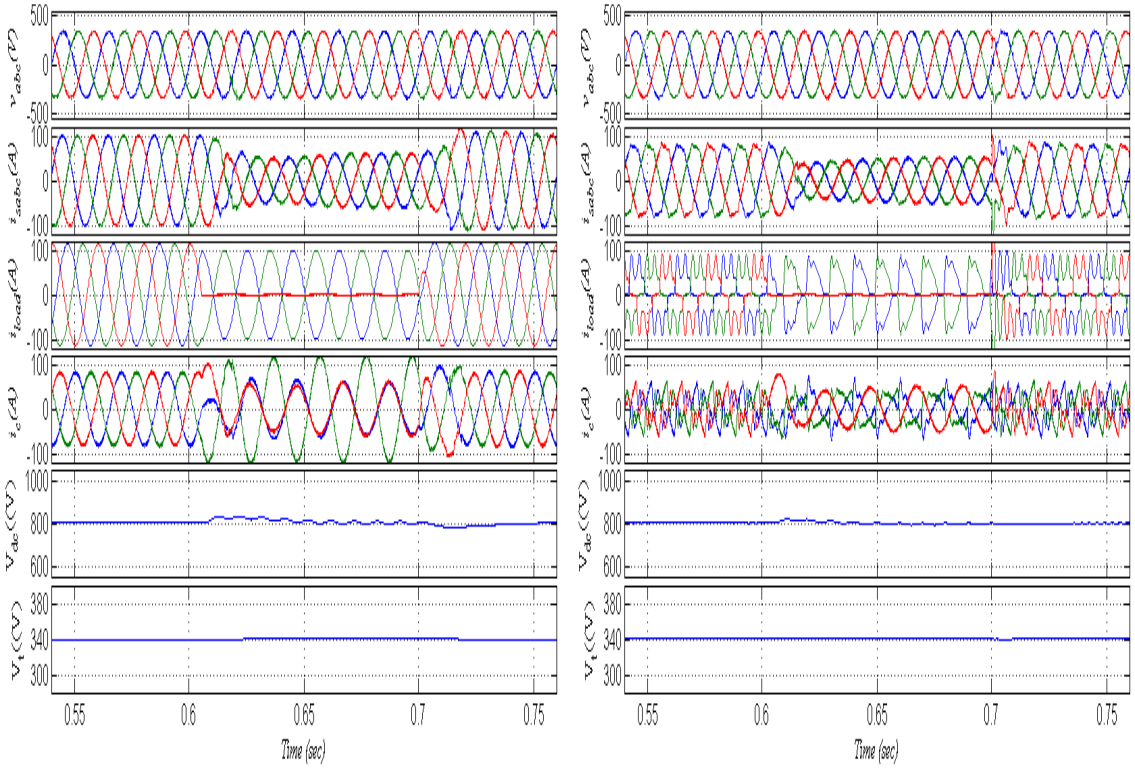
Figs. 8(a)-(c) show the magnitudes of the source currents and Fig. 8(h) shows the voltage of phase A with the three phase source currents which are balanced while Figs. 8(d)-(f) show the magnitudes of the load currents and in one phase (phase C), current is very less (Fig. 8(f)). Fig. 8(i) shows the voltage of phase A with the three

phase unbalanced load currents. The source currents are balanced and in phase with voltage because unbalanced load current are compensated by DSTATCOM currents (Fig. 8(j)). THD of source currents of phase A in steady state is 4.4 % as shown in Figs. 8(g).

5.3 performance of the dstatcom with nonlinear load

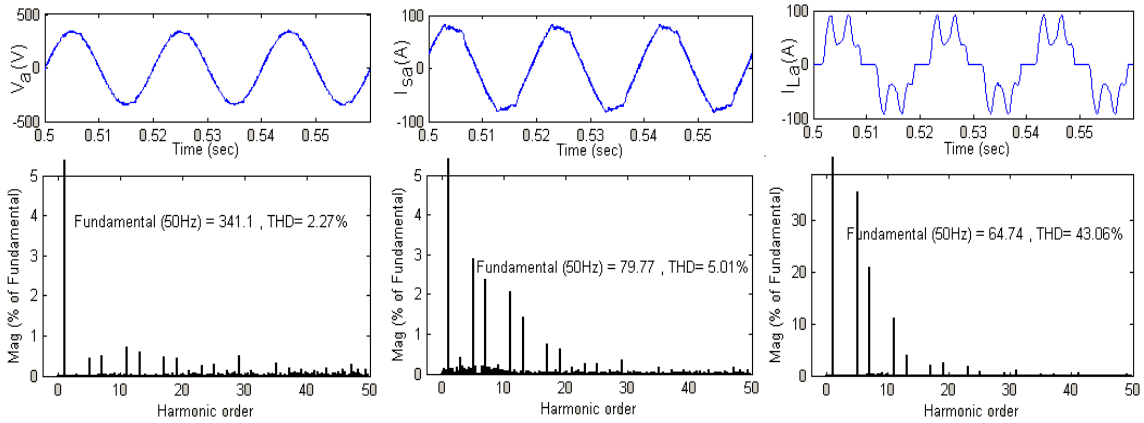
Figs. 9(a) and (b) show the source current of phase A and load current of phase A as shown in Fig. 9(a), the source current is sinusoidal while the load current shown in Fig. 9(b) shows the load is non linear. The THD of nonlinear load is 27.7% but the harmonic is eliminated by the DSTATCOM and the THD on Source side is reduced to 3.6%. The harmonic spectra of source current and load current is shown in Fig. 9(c) and Fig.9(d). Fig. 9(e) shows the source voltage, source current, load current and DSTATCOM current of phase A. The load current content harmonics while source current is sinusoidal, in phase of source voltage and harmonics free as the harmonics are eliminated by injecting the harmonic current using the DSTATCOM.

The starting response of the DSTATCOM is shown in Fig. 9(f). As the DSTATCOM is switched ON, the DC Bus voltage of DSTATCOM is start to build up to its reference value i.e. 200V and at the same time controller respond to eliminate the harmonic current from the source current which shows that the control algorithm is fast and DC bus voltage is also stabilized within one cycle of source frequency.



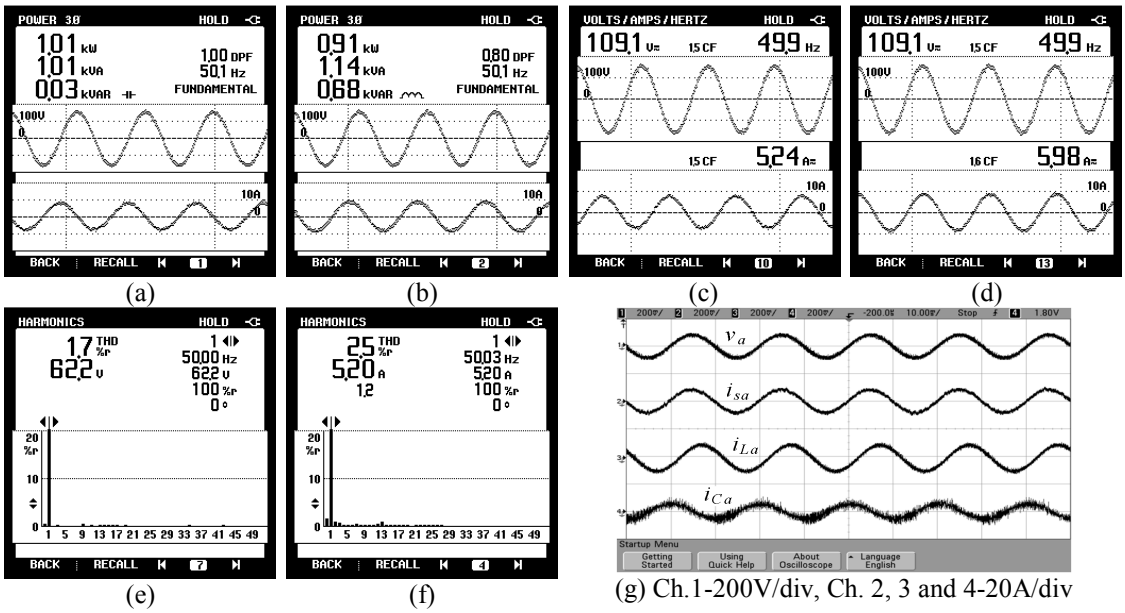
(a) (b)

Fig. 5. Performance of DSTATCOM in ZVR mode controlled by modified IcosΦ algorithm (a)with linear reactive load (b)with nonlinear load.



(a) (b) (c)

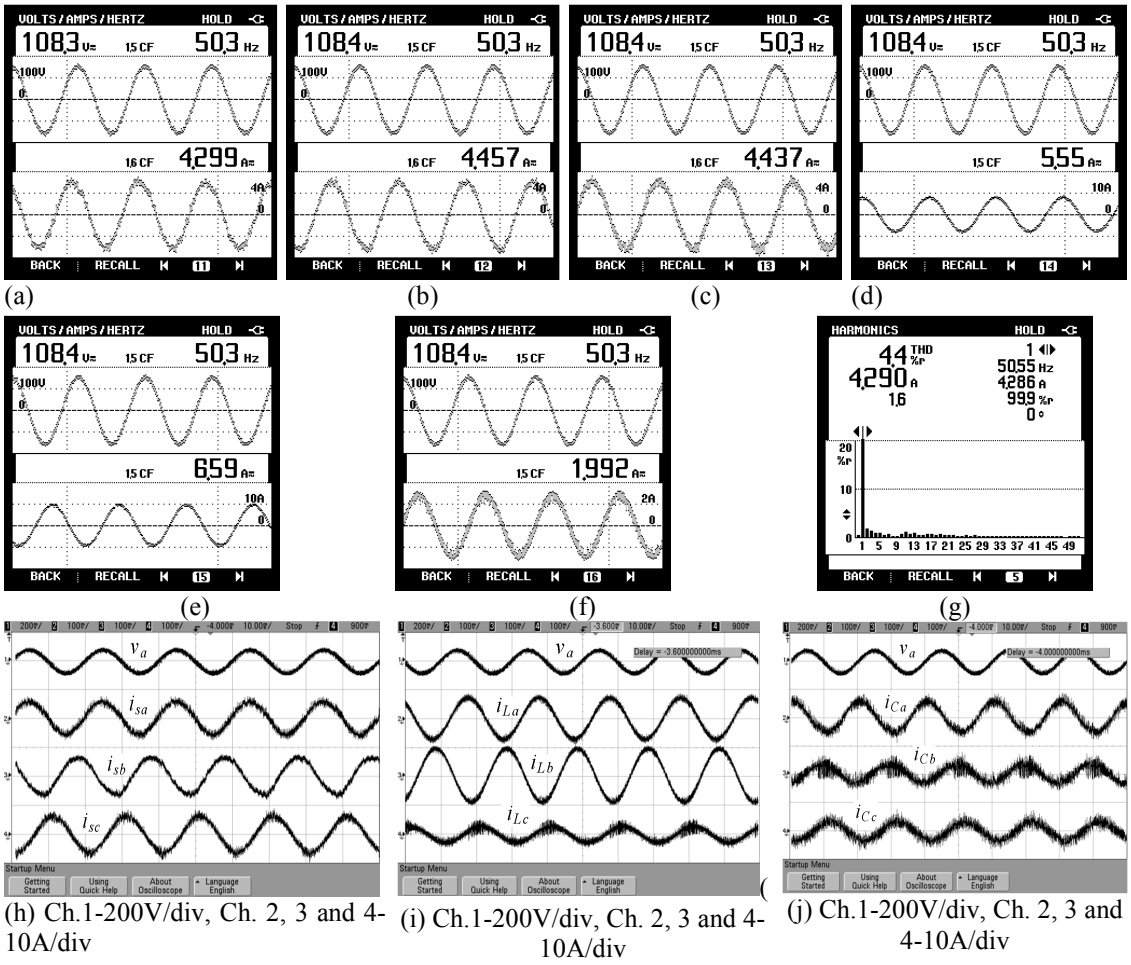
Figs. 6. Waveform and THD spectrum of (a)PCC voltage of phase A (b)source current of phase A (c)load current of phase A in ZVR mode.



(a) (b) (c) (d)

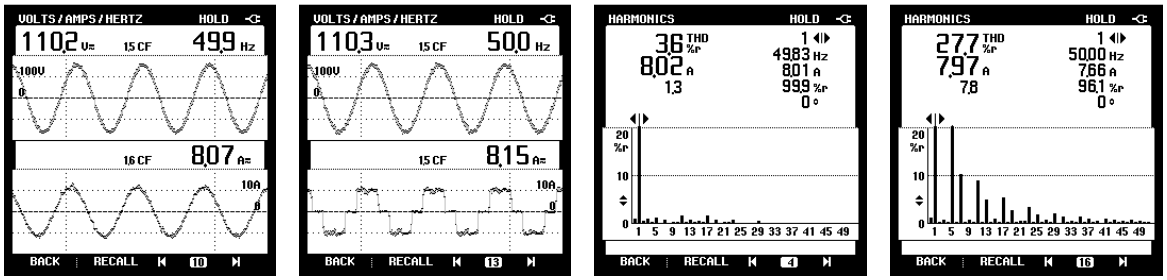
(e) (f) (g) Ch.1-200V/div, Ch. 2, 3 and 4-20A/div

Fig. 7. Performance of the DSTATCOM with a balanced lagging pf linear load (a)source side power and Power factor (b)load side power and Power factor (c)PCC voltage and source current (d)load side voltage and current (e)PCC voltage THD (f)source current THD (g)PCC voltage source current, load current and DSTATCOM current of phase A.

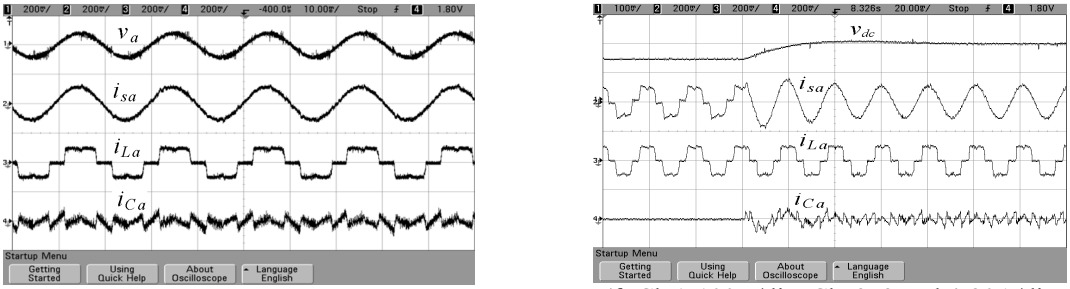


(h) Ch.1-200V/div, Ch. 2, 3 and 4-10A/div (i) Ch.1-200V/div, Ch. 2, 3 and 4-10A/div (j) Ch.1-200V/div, Ch. 2, 3 and 4-10A/div

Fig. 8. Performance of the DSTATCOM with an unbalanced linear load (a)PCC voltage and source current of phase A (b)PCC voltage and source current of phase B (c)PCC voltage and source current of phase C (d)PCC voltage and load current of phase A (e)PCC voltage and load current of phase B (f)PCC voltage and load current of phase C (g)source current THD (h)PCC voltage (phase A) and three phase source currents (i)PCC voltage (phase A) and three phase load currents (j)PCC voltage (phase A) and three phase DSTATCOM currents.



(a) (b) (c) (d)



(e) Ch.1-200V/div, Ch. 2, 3 and 4-20A/div (f) Ch.1-100V/div, Ch. 2, 3 and 4-20A/div

Fig. 9. Performance of the DSTATCOM with a nonlinear load (a)PCC voltage and source current (b)PCC voltage and load current (c)source current THD (d)Load current THD (e)PCC voltage, source current, load current and DSTATCOM current of phase A (f)DC bus voltage, source current, load current and DSTATCOM current of phase A.

6. CONCLUSION

The simulation and implementation of DSTATCOM with the modified *IcosΦ* algorithm have been carried out for the compensation of linear balanced/ unbalanced load and nonlinear load in three phase three wire distribution system. The power factor correction mode and voltage regulation mode of DSTATCOM have been achieved for load compensation with modified *IcosΦ* algorithm. The DC bus voltage of DSTATCOM has been regulated to its reference value for various loading conditions. In simulation, it is found that the performance and response of controller is fast and effective in both power factor correction mode and voltage regulation mode for compensating the linear balanced/ unbalanced load and nonlinear load. In hardware, load balancing and harmonic elimination is also achieved and the response of controller to compensate the load is found effective and fast.

Appendices

A) data for simulation

AC line voltage 415V (L-L), 50Hz; source impedance: R_s=0.02Ω, L_s=0.4mH; voltage source converter: DC link voltage 800V, DC capacitor 10000μF, interfacing inductor 2.3mH, switching frequency 10 kHz. For ripple filter: R_r =*3.5*Ω, C_r=18μF; linear load: 3 phase load 46kW, 0.8 pf lag each, nonlinear load: 3 phase bridge rectifier with R =*9*Ω, C=220μF, K_{pd}=1.7, K_{id}=2.5, K_{pa}=20, K_{ia}=35.

B) data for hardware implementation

AC line voltage 110V, 50Hz; VSC: DC bus voltage 200V, DC bus capacitor 1650μF, interfacing inductance 3mH, switching frequency 10 kHz, 5-Hall effect current sensors (ABB EL50 P1 BB) and 3-Hall effect voltage sensors (ABB EM010 BBFHPIN).

7. REFERENCE

R. C. Dugan, M. F. McGranaghan and H. W. Beaty, *Electric Power Systems Quality*. 2ed Edition, McGraw Hill, New York, 2006.

K. R. Padiyar, "*FACTS Controllers in Power Transmission and Distribution,*" New Age International (P) Limited, Publishers, New Delhi, 2007.

H. Akagi, E.H. Watanable and M. Aredes, "*Instantaneous power theory and application to power conditioning,*" Jhon Wiley & sons, New Jersey, USA, 2007.

Antonio Moreno-Munoz, *Power Quality: Mitigation Technologies in a Distributed Environment*, Springer-Verlag London limited, London, 2007.

Angelo Baggini, "Handbook on power quality," John Wiley & Sons, New Jersey, USA, 2008.

P. Jayaprakash, B. Singh, and D.P. Kothari, "Three-Phase 4-Wire DSTATCOM Based on H-Bridge VSC

with a Star/Hexagon Transformer for Power Quality Improvement," in *Proc. of ICIIS 2008*, Dec. 2008, pp.1-6.

B. Singh, P. Jayaprakash, and D.P. Kothari, "Three-phase four-wire dstatcom with H-bridge VSC and star/delta transformer for power quality improvement," in *Proc. of INDICON 2008*, Vol. 2, Dec. 2008, pp.412 - 417.

Soo-Young Jung, Tae-Hyun Kim, Seung-Il Moon and Byung-Moon Han, "Analysis and control of DSTATCOM for a line voltage regulation," *in Proc. of IEEE Power Engineering Society Winter Meeting,* Vol. 2, 2002, pp.729 - 734.

Bhim Singh, S. S. Murthy, and Sushma Gupta, "Analysis and design of STATCOM-Based Voltage Regulator for Self-Excited Induction Generators", *IEEE Trans. Energy Conversion*, vol. 4, dec.2004, pp783-790.

G. Bhuvaneswari and M.G. Nair , "Design, Simulation and AnalogCircuit Implementation of a Three-phase Shunt Active Filter using the Icosφ Algorithm,"*Conf. IEEE PEDS '05,* vol. 1, Jan. 2006, pp. 553 –55.

G. Bhuvaneswari, M.G. Nair and S. Kumar Reddy, "Comparison of Synchronous Detection and IcosΦ Shunt Active Filtering Algorithms,"*Conf. IEEE PEDES '06*. , Dec. 2006, pp. 1 – 5.

G. Bhuvaneswari and M.G. Nair, "Design, Simulation, and Analog Circuit Implementation of a Three-Phase Shunt Active Filter Using the IcosΦ Algorithm," *IEEE Trans. on Power Delivery*, Volume 23, pp. 1222 – 1235, April 2008.

Bhim Singh and Sunil Kumar, "Control of DSTATCOM using IcosΦ Algorithm," *Conf. IEEE IECON'09,* 2009, pp. 322–327.