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Design of Delta Sigma Modulators for Integrated Sensor Applications

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Abstract
The paper presents and explores the implementation of Delta Sigma Modulators for Integrated sensor applications. Elaborate design procedures and trade-offs faced have been presented. Starting at the block and topology level, comparisons of various feasible choices have been presented, along with the suited applications. Circuit level comparisons and trade-offs such as OTA and comparator design have also been presented. Finally, simulations have been shown for a modulator designed as per above criteria for integrated accelerometer applications.
Keywords: MEMS, Delta Sigma Modulators, Dynamic Range, Integrated sensors

1. INTRODUCTION

Integrated sensors like MEMS and NEMS have been gaining significant attention in the recent few years. The basic advantage with such sensors lies in their integrability with the current silicon technology, making miniaturization an easy goal. Such sensors find wide applications, specifically in high precision applications such as biomedical instrumentation, automobile industry and advanced sensing. The signal conditioning for such sensors is often on chip to reduce effect of parasitics. Typical requirements faced by the designer hence are high dynamic range and reproducibility. Serving as the front-end for on-chip high precision sensor applications, ADCs are widely used mixed signal blocks serving the purpose of transforming the noise prone and delicate analog outputs into robust and noise-immune digital binary outputs. With the advanced analog circuitry being implemented in digitally driven CMOS technologies, these are also implemented in the same technology. The rapid scaling in CMOS technologies has made supply voltages scale down to near 1V, which impels the use of simpler structures and blocks in such implementations [3]. Lower supply voltages further impel the designer to strategically lower the noise floor in an attempt to maintain a feasible dynamic range. The design requirements are also, apart from low chip area and power, to keep a robust, digital output capable of being transmitted to a remote master. Integrated sensors being low bandwidth systems typically [5], this remains to be the only parameter that can be traded-off. Various ADCs can be implemented for the purpose, each with its set of trade-offs and advantages. $\sum \Delta$ ADCs are however most widely accepted and suited for such high resolution applications. The advantage with these lie in their inherently high linearity owing to low-bit quantizer and feedback type implementation. Further, $\sum \Delta$ ADCs have relaxed design constraints for major building blocks [2], which adds to the ease of implementing the same. Modern CMOS technologies however present the challenges of reduced signal swing owing to low voltage environments along with low gain per transistor [1], [3] which necessitates special design techniques to overcome such constraints such as non-linearities in blocks and low finite OTA gain in nanometer CMOS technologies. The paper presents design techniques for $\sum \Delta$ ADCs in such integrated sensor applications. Section II discusses the block level specifications such as order, topology design and implementations. Section III presents constraints imposed by the process chosen, the secondary level topology design such as integrator and DAC designs, as well as transistor level designs for various sub-blocks, under the constraints imposed by the process, specifically in correspondence with low nanometer CMOS switched capacitor implementations. Chip level constraints owing to mixed signal designs have also been presented in Section III. Section IV finally presents the simulation results for one such modulator designed for an integrated accelerometer signal conditioning.

2. SENSOR INTERFACING AND BLOCK LEVEL SPECIFICATIONS

Modern integrated sensors typically employ a monolithic fabrication with sensor and the signal conditioning located on the same substrate. The front-end typically functions to support the analog output to face the relatively harsh situations outside the chip. An ADC is ideally suited and typically employed for the purpose and

has been traditionally employed [5], [6]. Further, the advantage with single bit output also lies with the facility of being able to give feedback to the sensor for closed loop high precision applications [6], [19]. The block diagram for such an application is given as in Fig. 1, wherein the conventional ADC has been replaced by a cheaper, high resolution single bit modulator and an off-chip decimator. The latter performs the dual function of giving multi-bit outputs and filtering out the high frequency shaped noise generated by the modulator. This is conventional to all ∑ Δ ADCs. The present work hereafter focuses on the block level as well as the VLSI design of the former, since the latter is a digital filter and can be easily implemented [18]. The sensor employed in such applications is typically a low frequency device with bandwidths in orders of kiloHertz, and decides upon the bandwidth of the ADC desired. The signal input specifications are given by the on chip signal conditioning circuit as in Fig. 1. More elaborate specifications for the modulator are discussed further in this section. A basic ∑ Δ modulator topology is presented in Fig. 2. The modulator consists of integrator and comparator in feedforward with a DAC feedback. The closed loop transfer function performs to gain over signal to noise ratio using twofold mechanisms, viz oversampling and noise shaping, which is inherent to the feedback nature of the modulator [4]. Signal to Noise ratio (SNR) for such a modulator is hence given as

$$SNR = 6.02 * log_2(OSR) + 1.76\,dB \quad (1)$$

for a first order modulator. Here OSR is the Over-Sampling Ratio given as

$$OSR = f_{sampling} / [2 * f_{bandwidth}] \quad (2)$$

The SNR increases with increase in modulator order. Complexity of the modulator also increases with the same. An elaborate study of such modulators has been presented in [2], [4].

2.1 Modulator Order and OSR

∑ Δ modulators of increasing order and complexity can be used to develop finer designs. The order of the modulator should be decided by the bandwidth requirements and the OSR hence achievable. First order modulators typically are used with OSR more than 512 to achieve any significant noise shaping. A lesser OSR demands a higher order topology to achieve the same SNR. A still lower OSR will further require a higher bit quantizer and a higher complexity DAC as well. The latter is however, not preferred in literature owing to increased complexity and errors in multi bit quantizers. Further, it should be noted that stability as well as input signal swing of ∑ Δ modulators decreases rapidly with increasing orders [2]. A first order modulator is inherently stable owing to simplicity in realization, and also supports a rail to rail input. Signal swing constraints increase in second order realizations, where input swing is limited to 70% of the rails. Various ways have been developed to overcome these constraints, but compromise on other aspects like stability and complexity [2]. Modulators beyond 5th order are not found in literature due to above constraints. A trade-off may be decided based on elaborate simulations in pre-developed toolboxes [2], [9]–[11]. Modulator order largely depends upon the noise shaping desired in the same. A basic topology as in Fig. 2 will result in a 20 dB/decade noise shaping, while higher topologies in integral orders will lead to a more aggressive noise shaping in units of 20 dB/decade. Higher noise shaping also means more low-frequency noise suppression in the pass band, and hence an increased SNR. However, increase in order also results in an increased instability and decreased signal swing, as mentioned above. Topologies hence need to be modified as per the trade-off and the application desired. A summary of such topologies for second order modulators can be found in [2]. Further, since higher order modulators lead to instability, often cascading of lower order modulators is preferred over single higher order modulator to achieve the desired attenuation. Sensor applications prone to near-dc noise need a band-pass modulator topology, wherein the signal transfer function assumes a band pass characteristic compared to the conventional low pass ones. The low frequency noise suppression can be decided by the dynamic range desirable from the modulator. The sampling frequency can be decided using the sampling required at the analog back-end, hence defining the OSR. First order modulators are the most stable and offer rail to rail input swing. However, it is to be noted that they also introduce a significant amount of nonlinear effects and coloured noise, recognized in literature as idle tones, owing to their correlations between input signal and the quantization noise [7]. There is further also an effect of input signal frequency [2]. These are not preferred, unless the modulator is to be operated at very high oversampling ratios. Generally, OSR for such modulators is more than 512. The advantage, however, is low chip area, complexity and power consumption.

2.2 Modulator Topology and Implementations

∑ Δ modulators with higher orders may be implemented in variety or topologies, broadly categorized as feed-forward and feedback topologies. A major consideration in deciding the topology is the noise transfer function desired, since this is the main factor altering SNR. The signal transfer function may then be a low pass or a band pass filter, depending upon the application desired. The former is used in sensor applications and flip-over capacitor implementations, while the latter is more implemented for telecommunication applications. Once the order and the OSR for the modulator have been decided, topology and its stability can be predicted using elaborate simulations [11], [12]. Non ideal inclusions such as finite op-amp gain and noises in blocks can be

implemented in the same using [10]. This is especially useful when assessing the performance of the modulator compared to ideal one, and to arrive at a trade-off hence.

The implementations may be done in a variety of ways. Continuous time implementations typically require passive component realization, not all of which can be easily achieved. Discrete time implementations such as switched capacitor and flip-over implementations offer the advantage of easy integrability with modern CMOS technologies, more precision in component realization and added programmability feature. CMOS technologies further prefer a fully differential implementation topology against a single ended one owing to 6 dB increased dynamic range and common mode noise attenuation, typically required for discrete time and mixed signal applications [4], [8]. However, single ended implementations, being simpler, are also found in the literature [13].

3. CIRCUIT LEVEL SPECIFICATIONS

A. Process

Modern CMOS process tend towards low nanometer feature sizes, resulting in decreased supply voltages. This imposes several constraints on the modulator design. Firstly, the blocks hence to be realized need to be operable at low voltages, while giving a significant signal swing. Secondly, the dynamic range offered by the blocks should be desirably high, which demands to lower the noise floor. Design considerations hence typically include low voltage opamp design and comparator design. Thirdly, the design, if using a unipolar supply, needs to be built around a common mode voltage, which directly determines the signal swing and hence the dynamic range. It hence needs to be judiciously chosen, and is generally kept to mid rail in attempt to optimize signal swing. [3], [13] give examples where such a generalization is violated, owing to op-amp constraints and power optimizations.

B. Integrator Topology

The integrator here acts with feedback to add or subtract the common mode from the input signal based upon the current modulator output, thus performing the dual function of feedback summing and integration. The feedback mechanism is critical to such implementations hence, apart from considerations to integrator design. It should be further noted that input capacitance needs to be kept large, typically more than 1 pF, and closely matched, to avoid and minimize any mismatch errors. This is especially critical since any mismatch in these capacitors directly affects the gain in both the legs, and appears as a differential error not reject-able by the circuit. The same applies to the switches used in the path.

1) Integrator Feedback Mechanism, DAC and Switch Design:

The feedback to the integrator may be given directly through the output [5], or indirectly using switches [3]. The former topology charges the input capacitance directly through the comparator output, while the latter one only takes signal from the output to trigger the switches accordingly. The former hence requires comparators large enough to be able to drive the input capacitance, inherently set high. This increases both power requirement and area requirement for the comparator. Further, there are slew rate limitations with the former topology owing to comparator based charging. The latter instead uses an indirect feedback, wherein output signals the switches to connect the feedback node to signal high or or signal low voltage. This effectively eliminates the errors due to comparator designs, though pushing the same to switches employed in the task. Though indirect, the latter topology is more advantageous and preferable, provided switches are suitably designed.

The switches can be sized by arriving at a trade-off between signal attenuation and switching errors. Since both rails may need to be transmitted, the switches typically are designed using a pass transistor topology. Local inverters can be used for driving both the transistors, giving two-fold advantage of reducing capacitive loading on clock as well as errors due to variations in clock voltages over the chip, and disturbance of clock owing to other switchings. The pass transistors have to be further designed to give a suitable frequency response at the desired capacitive loading. A large capacitive loading here will reduce voltage errors due to charge injection. However, driving large loads will also require larger pass transistors, which will in turn increase charge injection errors. A trade-off hence needs to be decided judiciously using elaborate simulations. Frequency response of the switches for the given capacitive loads should be flat to the frequency range desired.

2) OTA Type Selection:

Signal swing at the integrator output directly determines the dynamic range for the system, as given by the following expression [3]

$$DR = V_{in,max} * OSR * C_{Sampling}/2 * k * T \quad (3)$$

Here DR represents the dynamic range, $C_{Sampling}$ represents the initial sampling capacitor, and T represents the temperature in Kelvin. It is desirable from (3) that the OTA has rail to rail output swing, with low noise floor. Further, the gain requirements from the OTA are given as [14]

$$A_0 > [C_{Sampling}/C_{Integration}] * [OSR/\pi] \quad (4)$$

$C_{Integration}$ here represents the feedback capacitor in the integrator configuration. Apart from giving the minimum gain constraints, (4) also gives the consequence of high OSR on OTA gain. The gain requirements increase with OSR and overall intergator gain. It is desirable then, that OSR be kept low enough to have an achievable gain. This is especially critical to modern CMOS technologies since gain per transistor decreases in low nanometer ranges [3].

It is also expressed herein by (3) that the noise floor be kept minimum in order to optimize the dynamic range. This can be effectively done by avoiding use of noisy components like resistors in opamp design, since they typically have a larger noise floor than capacitors. Among the prominent topologies, folded cascode poses power consumption and area problem, still giving lower signal swing and hence dynamic range. A better choice is offered by current mirror OTA with rail to rail output [3]. The minimum operating voltage required for the same is suited to low nanometer designs, given as

$$V_{DD,min} = V_T + 3V_{Dsat} \quad (5)$$

On the other hand, the dynamic range is optimized by rail to rail swing. Being single stage compensation-less design, it further gives low power consumption. Gain enhancement is generally employed since the OTA gain in itself is low. A tradeoff generally needs to be done between phase margin and output driving capacitors. These OTAs generally hence require a high output capacitance to give stable phase margins.

A Common mode feedback circuit needs to be incorporated in the OTA for stabilizing the common mode voltage required in unipolar environment. The same is discussed in Section 3.5.

C. ADC Selection

The comparator in Fig. 2 acts as the 1 bit ADC. The same may be implemented using a traditional OTA based design or a dynamic comparator based design.

1) Uncompensated OTA based ADC:

In [15], elaborate design procedures for designing such a comparator are presented. It is essentially same as OTA design but without any compensation. It should be noted that such a comparator hence occupies significant static power and chip area. It is preferable in low frequency applications owing to simplicity. It is further important to be noted that symmetrical limbs of the comparator need to be closely matched to avoid offset errors and hence SNR degradation. Of prominent importance are the input transistors, matching of which directly reduces the comparator offset.

2) Dynamic Latch based ADC:

In [17], a comparator topology for high speed designs is presented based on dynamic preset latches. The operation of the same is governed by the resistances offered by the input transistors, which is directly dependent upon the gate voltages of the transistors. Though it is important in this topology that the latches be matched, the matching of input transistors is most critical here since they are the main decision making devices. Since the comparator has a reset pre-charge phase, it needs to be followed by a suitable latch in order to keep the output stable during the pre-charge phase. A major advantage of this comparator is zero static power consumption owing to digital latch based design. Chip area is further an advantage.

D. Non Overlapping Clock Generator

1) Traditional Type:

Owing to switched capacitor design, the VLSI implementation of the modulator requires perfectly non-overlapping clocks to switch the required capacitors. The requirement is that the complementary phase should not rise till the first phase has settled to zero. The simplest traditional development for the same is given as in Fig. 3. Here, as can be observed, the complementary phase cannot rise till the first phase has settled, owing to NAND gate latch-like design. Phases P1 and P2 form the complementary phases, with the non-overlap delay controlled by the overlap control inverter chain. The inverter chain should have a sufficient delay for the required performance to be achieved. The delay required generally is based upon the operating clock, typically a small fraction of the clock time period. The delayed phases P1d and P2d produce delayed replicas of the two basic phases P1 and P2 respectively, while the delay may be controlled by the delay control inverter chain. Since digital outputs are available, the buffers used can be implemented using a simple increasing size inverter chain with even number of inverter stages. This may be necessary since the phases may be driving capacitive loadings imposed by the transistors being driven.

2) Bottom Plate Sampling type:

VLSI designers prefer use of bottom plate sampling based design for reducing charge injection errors due to CMOS switches in switched capacitor circuits [2], [3], [5]. The concept here is to disconnect the bottom plate of the switching capacitor before the top plate, disconnecting one terminal of the capacitor. The top plate can then be switched after a short delay with no voltage error owing to disconnected bottom plate. The same may be implemented using an advanced clock generating topology shown in Fig. 4. It gives delayed phases along with complimentary, non-overlapping phases. An inverter chain may be employed for obtaining a suitable delay in the delay controlling elements as in [5].

E. Biasing and Other Auxiliaries

Biasing for the OTAs and comparators in the circuit may be supplied using reference generators. Sensor applications typically require the signal conditioning to function under varying temperatures, and hence it is preferable to use a temperature independent reference. The OTA also requires a common mode input along with a common mode stabilization circuit commonly known as the common mode feedback circuit (CMFB). The CMFB may be continuous time or discrete time, depending upon the application desired. [5] employs a continuous time CMFB in folded cascode OTA design, while [3] prefers a switched capacitor based design. The advantage of the latter is owing to reduced chip area and zero static power consumption. It however, employs use of biasing voltage for generating required voltage for driving the CMFB transistors. It further, unlike its continuous time counterpart, also sinks current from the common mode generated. This further necessitates a common mode generator capable of sourcing the required current. Often, a low power unity gain amplifier following the common mode generating transistors may be employed for the same.

F. Layout Precautions

The layout precautions and techniques employed for analog as well as digital VLSI designs are applicable, though with added concern over their interactions in the common substrate environment, often called as the mixed signal design. The foremost is that the supplies for both the digital and the analog parts need to be separated in the chip, in order to avoid supply bounce in delicate analog circuitry due to rapid switchings in the relatively robust digital circuitry [3], [16]. Further, the analog and digital parts of the circuit should be laid out separately on the common substrate and separated by a guard ring to avoid interference between the two. Sensitive analog circuitry such as reference generator should be kept further from the digital part, while the more robust blocks such as the comparator can be kept closer, as shown in Fig. 5 illustrating the case of a first order modulator. Crossing of digital and analog lines should be avoided as far as possible, or should be shielded with a ground plate in the middle. The same applies to digital and analog lines passing close by in the same layer.

Contacts should be laid out in plenty to reduce resistances arising from them and also increase their reliability. On circuit level, the input transistors of the OTA and the comparator should be closely matched, often achieved by laying them out symmetrically close together or from a same transistor having multiple fingers. Dummy transistors or fingers may be placed to enhance matching. Interleaving of transistors may be done for current mirrors to enhance mirroring. The same may be done for resistances used in the reference generator. The differential limbs of the design should be symmetrically laid to avoid mismatches.

4.SIMULATION RESULTS

Design and simulation was performed for a first order modulator using above summarized rules in standard 180 nm CMOS technology. A simple temperature independent reference generator was employed with a switched capacitor CMFB. Results were obtained using a 15.625 kHz sine wave input with sampling clock set to 1 MHz, variable from 500 kHz up to 2 MHz. OSR hence achieved was 32, purposefully kept low for simulation results. Fig. 6 shows the transient performance of the circuit for a -1.58 dBFS, 1 kHz sine. Fig. 7 shows the output signal spectrum analyzed for a 0 dBFS, 500 Hz sine. The DFT data was obtained using the inbuilt Cadence DFT engine, while the logartithmic plot was obtained from MATLAB. As can be seen, a clear tone at the 500 Hz can be seen. There is also a 0 dBFS prominent tone observed at dc, corresponding to the common mode voltage, though the same has not been shown in the logarithmic x-axis. The other peaks correspond to spurs resulting due to non-linear effects of the modulator. Fig. 8 clearly shows the noise spectrum of the modulator, with a +20 dB/decade noise shaping. The same was obtained by removing the signal.

The low frequency noise floor was observed by carrying out DFT over multiple cycles. Further, since the DFT was carried out over an integral number of cycles, rectangular window was used, and hence the signal spectrum shows a single sharp tone, apart from the attenuated harmonic tones. Since the platform operated did not provide facilities for SNR calculation, the modulator performance was only relatively evaluated by observing the signal amplitude, the average noise floor and the harmonics. The latter, however, did not change much once the modulator topology and OTA gains were frozen. The design finalization fine-tunings were hence prominently carried out using the first two parameters. Outputs were observed for a large range of inputs for both practical and ideal case simulations. The DFT for 15 kHz sine was carried out over nine complete cycles, leading to results as summarized in Table I. As can be seen, the modulator gives desirably close amplitudes, and the maximum amplitude attenuation was about 37 mdBFS. The average noise floor stayed below -280 dB for the design.

5.CONCLUSION

Modulators constitute an important part of modern analog signal processing front-ends and ASICs. The elaborate design procedures, starting from derivation of block level specifications and requirements, were presented. VLSI design level criteria, trade-offs and layout precautions were also presented. Finally, a modulator designed on the

above guidelines was presented and observed to give an average noise floor of -350 dB and signal attenuation less than 120 mDBFS.

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Table 1 Simulation Results for Ideal and Practical Cases

Input Signal	Ideal Case DFT Tone	Practical Case DFT Tone
-19 dBFS	-19.08 dBFS	-19.12 dBFS
-5 dBFS	-	-5.39 dBFS
-3.52 dBFS	-	-3.54 dBFS
-1.02 dBFS	-1.03 dBFS	-1.06 dBFS
0 dBFS	-7 mdBFS	-37 mdBFS

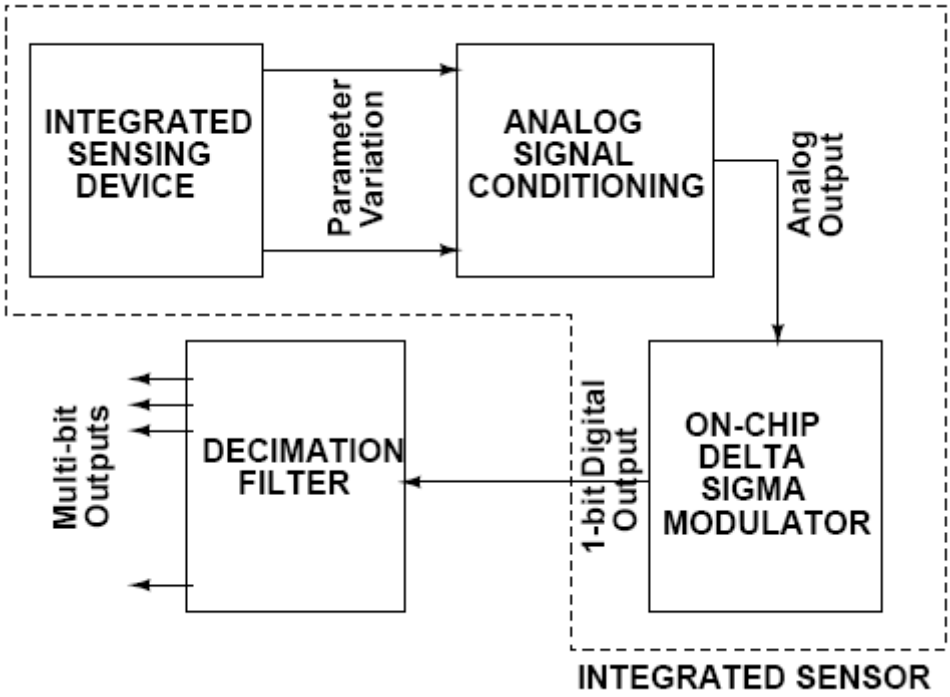

Figure 1 Integrated Sensor Basic Blocks using Delta Sigma Modulators

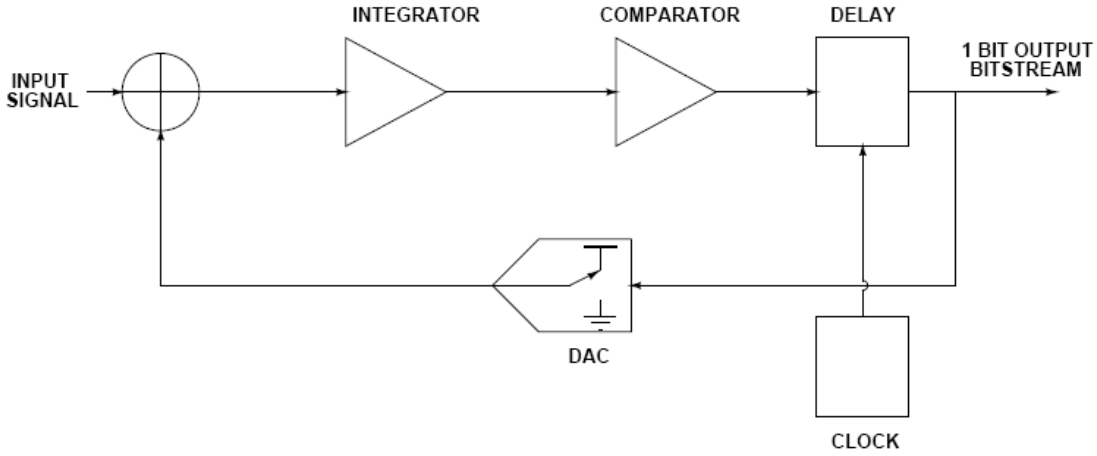

Figure 2 Basic First Order Delta Sigma Modulator

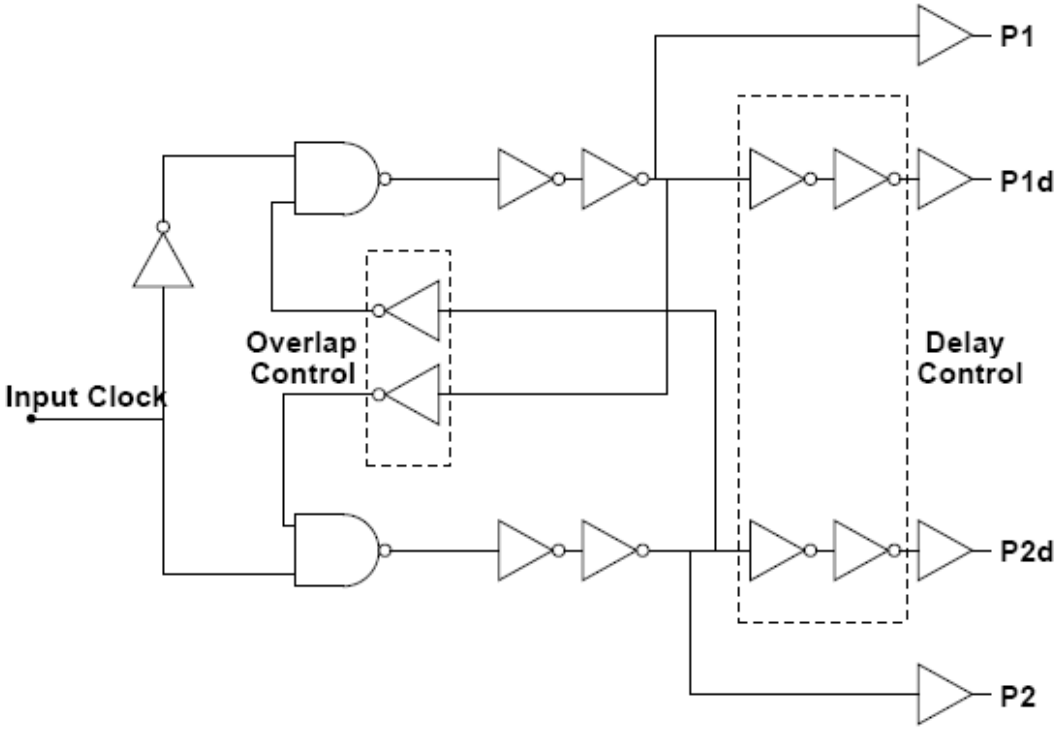

Figure 3 Basic Non overlapping clock generator

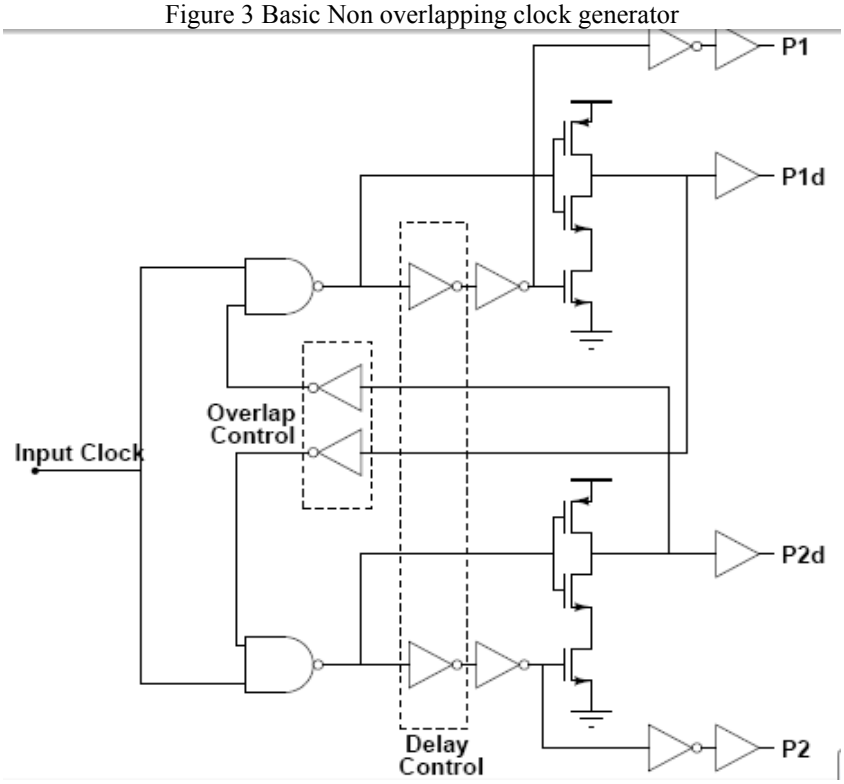

Figure 4 Non overlapping clock generator for Bottom Plate Sampling based designs

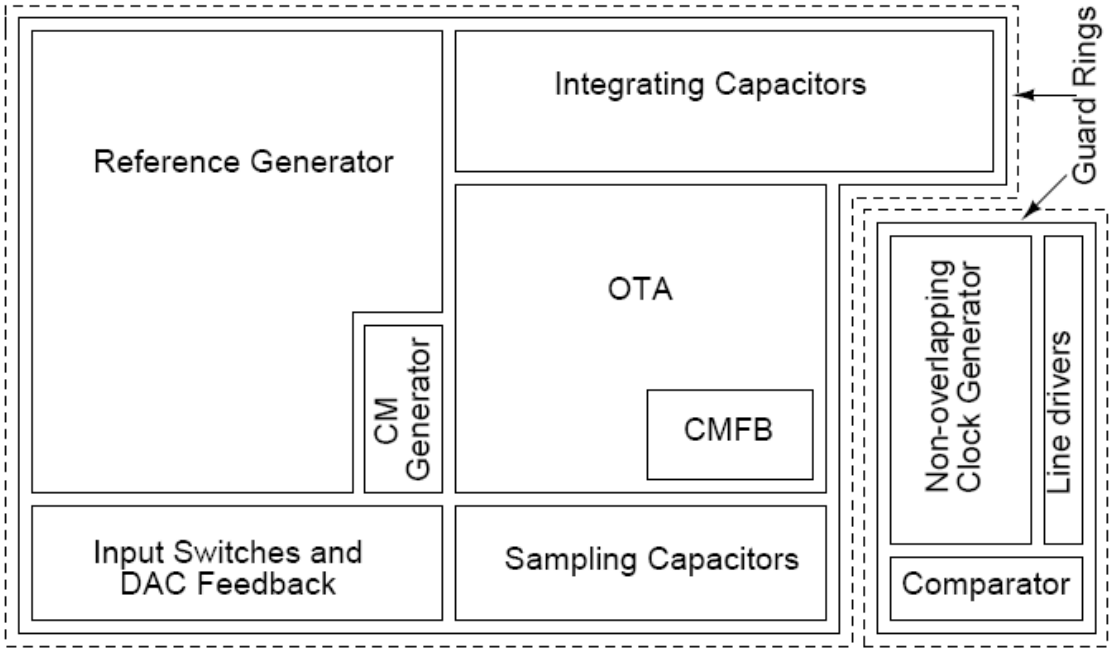

Figure 5 Sample Layout Plan for the modulator

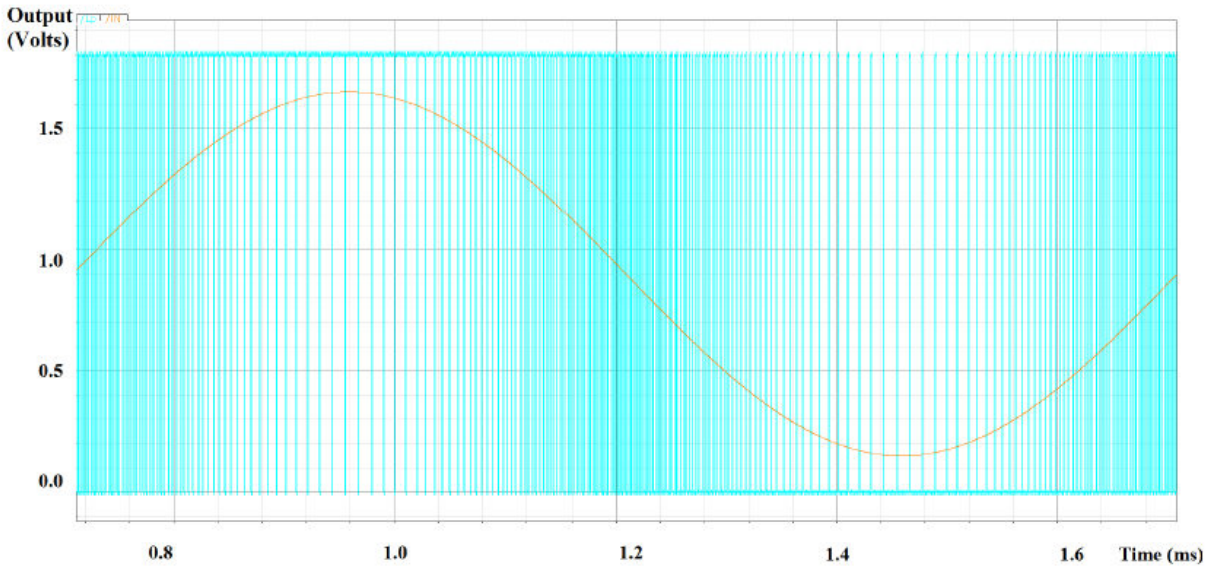

Figure 6 Simulated Output for the First Order Modulator

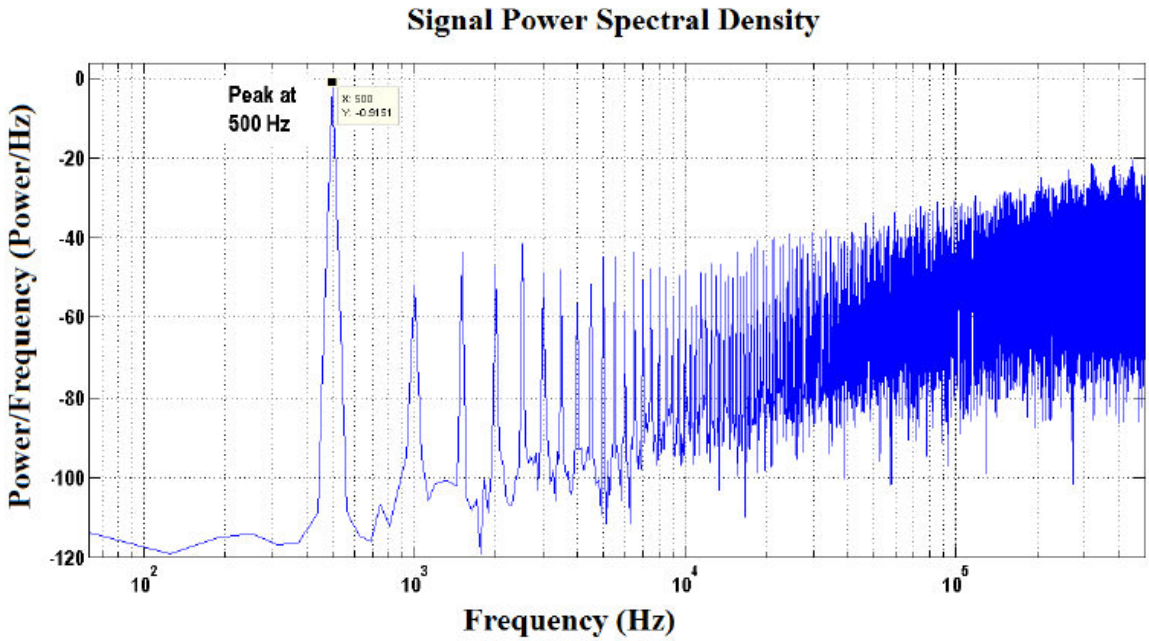

Figure 7 Output frequency content for a 500 Hz, 0 dBFS input to the modulator

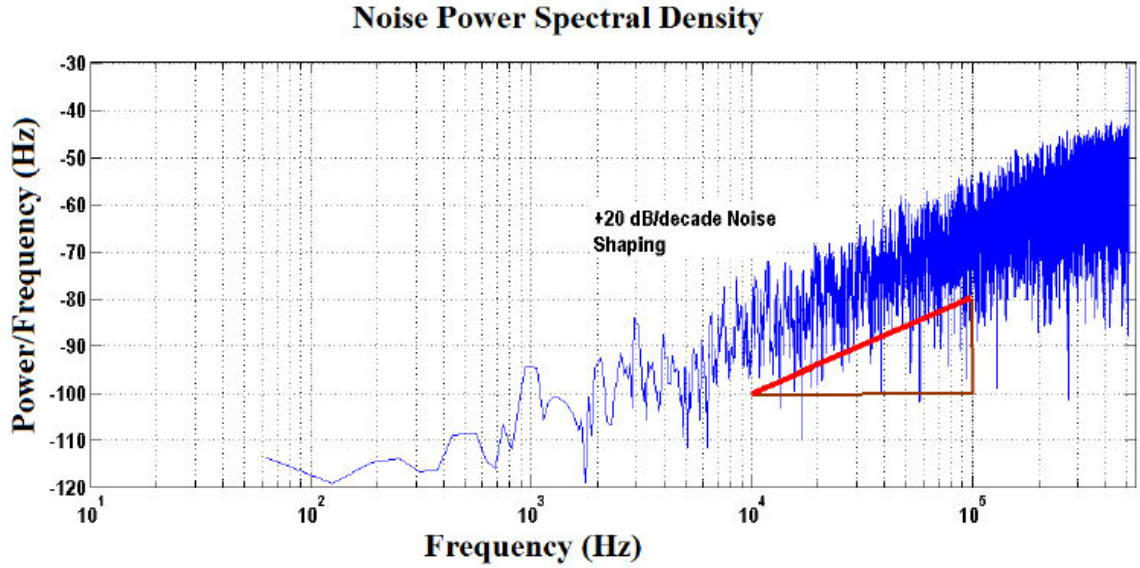

Figure 8 Noise content at the output of the