

Design of Ring Oscillator based VCO with Improved Performance

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Abstract

Voltage Controlled Oscillator plays significant role in communication system design. The design of Voltage Controlled Oscillator (VCO) with low power consumption and high frequency range is presented in this paper. The VCO is based on a single ended CMOS inverter ring oscillator**.** Accurate frequency of oscillation in Ring Oscillator is an important design issue. A Voltage Controlled Ring Oscillator with wide tuning range from 917.43MHz to 4189.53MHz can be achieved using bulk driven technique by varying the threshold voltage of the MOS circuits. The circuit is designed using 0.13µm CMOS process for a supply voltage of 1V. Simulation results show better accuracy compared to existing current staved ring VCO using different number of inverter stages**.**

Keywords: Bulk driven technique, CMOS Process, Ring Oscillator, Voltage Controlled Ring Oscillator, Inverter.

1. Introduction

In integrated circuits, Voltage Controlled Oscillator (VCO) plays an important role [A. Hajimiri and T. H. Lee (1999), A. Rezayee and K. Martin (2001), D. A. Johns and K. Martin (1997)]. The performance of Voltage Controlled Oscillator is of great importance for any telecommunication or data transmission network. It is most commonly used in clock recovery circuits in digital communication and onchip clock distribution etc [Hesieh Y. B. and Kao Y. H. (2008), Anand S. S.B. and Razavi B (2001)].

The VCOs can be designed as LC circuits and as Ring Oscillators (ROs). Ring oscillators are often used in high-speed digital circuits for clock generation. Several reasons justify this popularity; one of them is wide tuning range, which can be easily obtained with a ring oscillator and another reason is, its compatibility with digital CMOS technology. Along with these advantages it occupies substantially less area than LC oscillators.

For the research in this area, the design of ring oscillator still possesses difficulties because of the inherent nonlinear behavior.

Some mathematical equations have been derived for frequency of oscillation of the RO, using small signal analysis [P.M. Farahabadi , H. Miar – Naimi and A. Ebrahimzadeh (2009)]. A ring oscillator circuit is shown in Figure 1, where *N* is odd number and refers to the number of inverter stages.

The frequency of the oscillation f_{OSC} can be found as:

$$f_{OSC} = \frac{1}{2N\tau} \qquad [1]$$

where, τ is the delay of one inverter stage. A variable resistor is added at the input terminal of each inverter as shown in Figure 2. Since the MOS transistors in each inverter can be assumed as switches, it can be replaced by a resistance $1/G_m$ as shown in Figure 3.

If the transconductance G_m and parasitic capacitances C_G of nMOS and pMOS transistors are assumed to be equal, the delay of each inverter stage (τ) will be approximately given as:

$$\tau = \frac{C_G\left(1+G_m R_V\right)}{G_m} \qquad [2]$$

Finally, the oscillation frequency can be found as:

$$f_{OSC} = \frac{G_m}{2NC_G\left(1+G_m R_V\right)} \qquad [3]$$

Equation (3) shows that the oscillation frequency of ring VCO which depends on the values of transconductance G_m , resistance R_V and capacitance C_G. However, G_m and C_G are device parameters and assumed to be constant. Thus the oscillation frequency can be controlled by changing the value of R_V [P. M. Farahabadi, H. Miar – Naimi and A. Ebrahimzadeh (2009)]. The approach to achieve wide frequency range of the voltage-controlled ring oscillator is by controlling the resistance. It creates better chance to design wide tuning frequency range ring oscillator through the voltage controlled resistor [Meng-Lieh Sheu, Ta-Wei Lin, Wei-Hung Hsu (2005)].

Wireless application requires oscillator which must be tunable. There are two types of controlled oscillators these are voltage and current controlled. Current Controlled Oscillators have not gained wide popularity because the high Q resonators are subject to tuning problem. The oscillator becomes useless in high speed wireless application which requires fast and wide tuning range. Conventional VCO based on RO utilize bias current to control the frequency of oscillation. In its most standard form output frequency of VCO is a linear function of its input control voltage as given by Equation 4:

$$f_{out} = f_o + K_{VCO} V_{ctrl} \qquad [4]$$

Where, f_o is the free-running frequency of the VCO, V_{ctrl} is the input control voltage and K_{VCO} is the sensitivity or gain of the VCO which controls VCO's output frequency. V_{ctrl} is the input to the VCO that sets it to the desired frequency [Stephen Docking (2002)].

The feedback properties of RO based VCO using bulk driven technique is the main feature of this paper. The organization of the rest of the paper is as follows: Section 2 provides the derivation of frequency of oscillation of an N stage Ring Oscillator. The proposed circuit is discussed in section 3. Simulation results and transient characteristics are provided in section 4 and lastly section 5 presents conclusion.

2. Ring Oscillator Circuit

2.1 Frequency Equation

The oscillation period of RO is determined by treating the RO as a chain of delay stages of inverter, although several other methods are also used in practice. A linear model of the RO with three stages is shown in Figure 4. Each inverter stage adds delay. The rise/fall time is related to the time constant RC of the inverter stage where R is resistive load and C is the capacitive load for delay stage. The frequency of oscillation of RO can be obtained by satisfying the Barkhausen criteria of unity close loop gain and total phase shift of 2π around the loop. The open loop transfer function of Figure 4 using small signal linear model can be written as:

$$H(s) = \left[-g_m\left(R \parallel \frac{1}{sC}\right)\right]^N = (-1)^N \left(\frac{g_m R}{1+\frac{s}{\omega_o}}\right)^N \qquad [5]$$

Where g_m is transconductance, $\omega_0 = 1/RC$ defines the reciprocal of time Constant and N is number of delay stage in small signal model. The frequency of oscillation ω_{osc} is related to ω_0 by the Equation 6 as:

$$\omega_{OSC} = \omega_O \tan\frac{\pi}{N} \qquad [6]$$

2.2 Existing circuit

To make the circuit to be voltage controlled, the oscillation frequency must be controllable and it can be controlled by delay also. One way to control the delay is to control the amount of current available to charge or discharge the capacitive load of each stage [Muhammad Touqir Pasha and Mark Vesterbacka (2010)] [M. Shahriar Jahan and Jeremy H. Holleman (2010)]. This type of circuit is called a current starved inverter and is shown in Figure 5.

The current sources, M3 and M4, limit the current available to the inverter, M1 and M2. Hence the total output frequency is varied according to control voltage [P.M. Farahabadi, H. Miar – Naimi and A. Ebrahimzadeh (2009), Shruti Suman, Monika Bhardawaj & Prof. B.P.Singh (2012)]. The maximum charge and discharge current is controlled by the current source I_{ctrl}. If V_{ctrl} is increased, I_{ctrl} increases, which in turn increases the current through M4, therefore reduces the time to discharge the load capacitance of the next stage. Since the current through M13 mirrors the current through M3, the charging time is also decreased. Therefore, an increase in V_{ctrl} reduces delay time τ , and thereby increases the output frequency.

3. Proposed Method

In modern communication systems power consumption and frequency tuning are key performance metrics. Growing demand of portable devices like cellular phones, personal communication devices have drawn attention for the low power consumption. Total power consumption P_{total} in MOS logic circuits is given by the Equation 7 as:

$$P_{total} = P_s + P_d + P_{sc} \quad [7]$$

Where, P_s , P_d and P_{sc} are the static, dynamic and short circuit power dissipation respectivily. Dynamic power dissipation results from switching of load capacitance between two logics and depend on frequency of operation, whereas static power is contributed by the direct short circuit current path between supply voltage and ground which depends on leakage current. Leakage power dissipation results from leakage current that arise from substrate injection and sub-threshold current.

Controlling the bulk terminal of CMOS device offers improved performance in term of power dissipation .In VLSI design, power and delay are the figure of merit during the selection and implementation of a device in chip fabrication. [T. Sharma, K. G. Sharma, B. P. Singh, Neha Arora (2010)]. To reduce the standby leakage in CMOS circuits, a reverse body biasing is generally used.

The schematic view of proposed ring VCO is shown in Figure 6. In this circuit, output frequencies of VCO have been controlled by varying the reverse bias voltage which also provides significant improvement in power consumption. The power consumption is reduced because of reverse substrate bias voltage.

The body biasing is used to control threshold voltage V_t. The effect of substrate bias voltage V_{SB} on the channel can be most conveniently represented as a change in the threshold voltage V_t as given in the Equation 8 as:

$$V_t = V_{to} + \gamma\left(\sqrt{|V_{SB} - 2\phi_F|} - \sqrt{|2\phi_F|}\right) \quad [8]$$

Here, V_{to} is the zero-bias threshold voltage, γ refers to the body-effect coefficient, V_{SB} is substrate bias voltage and φ_F represents the quasi-Fermi potential [Kang, S and Leblebici (2003)]. By changing the substrate bias voltage, the threshold voltage of the circuit can be changed. Threshold voltage affects the drain current. The variation in drain current, changes drain to source resistance of pMOS and nMOS transistors. So charging and discharging times can be varied according to body bias voltage and output frequency has been controlled by control voltage that is same as the reverse bias voltage applied at bulk terminal. If control voltage increases the threshold voltage also increases and hence the drain current decreases also source to drain resistance increases. This results in a decrease in the output frequency. As delay stage increase, output frequency decreases and power consumption slightly increases.

4. Simulation Results

The simulations of the proposed and the existing designs have been performed using Tanner EDA Tool version 13.0. All the proposed design simulations are performed on 130nm CMOS technology. In order to investigate that proposed design is consuming low power and have high performance, simulations are carried out for power consumption and output frequency at increasing input voltage.

4.1 Simulation Results for Existing Three Stage Ring VCO

The extra pMOS and nMOS transistors added in series with the inverter as shown in Figure 5, which limits the current through the inverter. Hence the output frequency varied according to control voltage as given in Table I. This table indicates that the frequency is tuned from 338.98 MHz to 1208.73 MHz with the variation of control voltage from 0.5V to 3V. The power supply voltage is taken as 3V. The output frequency shows almost linear relationship with the control voltage in the given range.The output waveform of existing current starved three stages ring VCO is shown in Figure 7.

4.2 Simulation Results for Proposed Three Stage Ring VCO

In the proposed three stage ring VCO, reverse bias voltage is applied at bulk terminal of nMOS and pMOS transistors as shown in Figure 6(a). Hence the output frequencies of VCO have been controlled by varying the reverse bias voltage which also reduces power consumption. The output waveform of proposed three stages Ring VCO of Figure 6(a) is shown in Figure 8. Table II shows results for proposed three stages Ring VCO. Control voltage has been varied from 3.2V to 0.4V with corresponding output frequency from 917.43MHz to 4189.53 MHz with deviation in power consumption from 3.61 µW to 29.21 µW. We have selected this range of control voltage because output frequency shows linear behaviour in this range.The control voltage is varied in negative direction because of reverse body bias voltage.

4.3 Simulation Results for Proposed Five Stage Ring VCO

The output waveform of proposed five stages ring VCO of Figure 6(b) is shown in Figure 9. Table III shows results for proposed five stages Ring VCO. Control voltage has been varied from 3.2V to 0.4V with corresponding output frequency from 546.44 MHz to 2399.57 MHz with deviation in power consumption from 4.51 µW to 35.71 µW. As the delay stage increase output frequency decreases because the delay is increased.

4.4 Simulation Results for Proposed Seven Stage Ring VCO:

The output waveform of proposed seven stages Ring VCO of Figure 6(c) is shown in Figure 10. Table IV shows results for proposed seven stage Ring VCO. Control voltage has been varied from 3.2V to 0.4V with corresponding output frequency from 393.70 MHz to 1723.60 MHz with deviation in power consumption from 4.64 µW – 37.82 µW.

4.5 Comparative Analysis of Proposed Three, Five and Seven Stage Ring VCOs

Figure 11 and Figure 12 shows output frequency and power consumption variation with control voltage. It shows nearly liner relation between control voltage and frequency of oscillation. As control voltage increases output frequency and power consumption also increases. This also shows that as delay stage increase output frequency decrease and power consumption slightly increases. The three stage proposed ring VCO shows high frequency range as compared to five and seven stage ring VCO.

4.6 Performance Comparison of Existing and Proposed Three stage Ring VCOs

Table V shows the comparative analysis of existing current starved and proposed three stage Ring VCOs. Power consumption and output frequency of proposed three stage Ring VCO circuit has been compared with existing circuit. The proposed circuit shows better performance. Power consumption has been reduced and oscillation frequency also increases with reverse body bias.

5. Conclusion

Improved power efficient design of three, five and seven stages Ring VCOs are presented in this paper. The output frequency shows almost linear relationship with the control voltage. The proposed circuit shows wide frequency range and low power consumption over the range of control voltage. The performance of proposed three stage Ring VCO has been compared with existing Ring VCO. Proposed three stage Ring VCO shows better performance in terms of power consumption and frequency range.

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He is life member of Indian Society for Technical Education (ISTE), New Delhi. His research interests are in the areas of reduced order modelling, VLSI circuits & devices, wireless communications and signal processing.

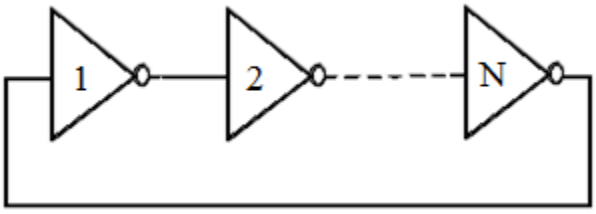


Figure 1. Single ended Ring Oscillator

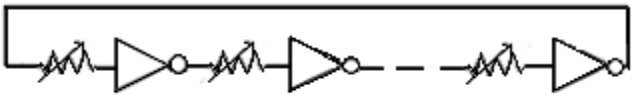


Figure 2. Circuit of Voltage Controlled Ring Oscillator

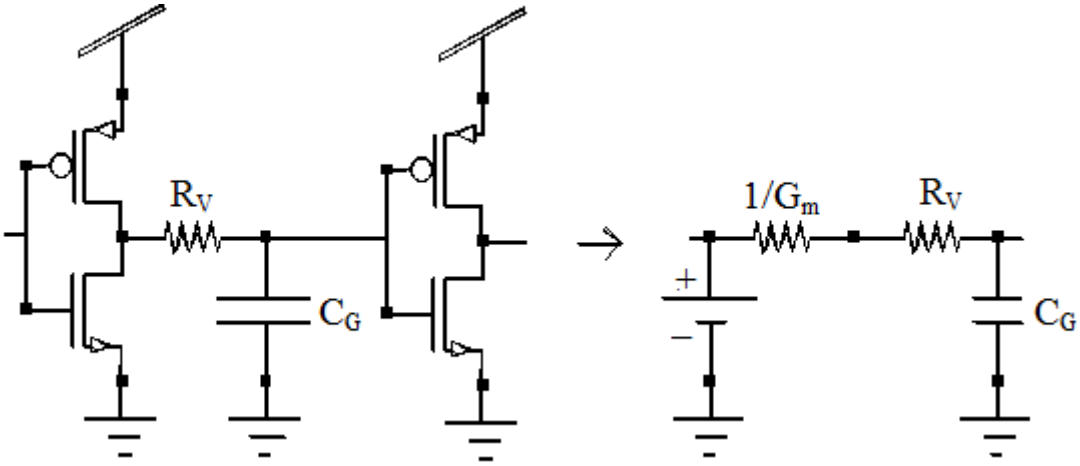


Figure 3. Delay approximation

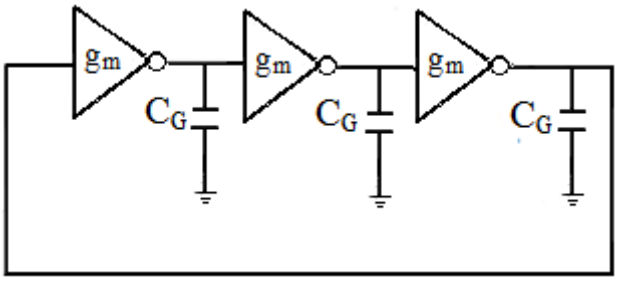


Figure 4. Linear model of ring oscillator

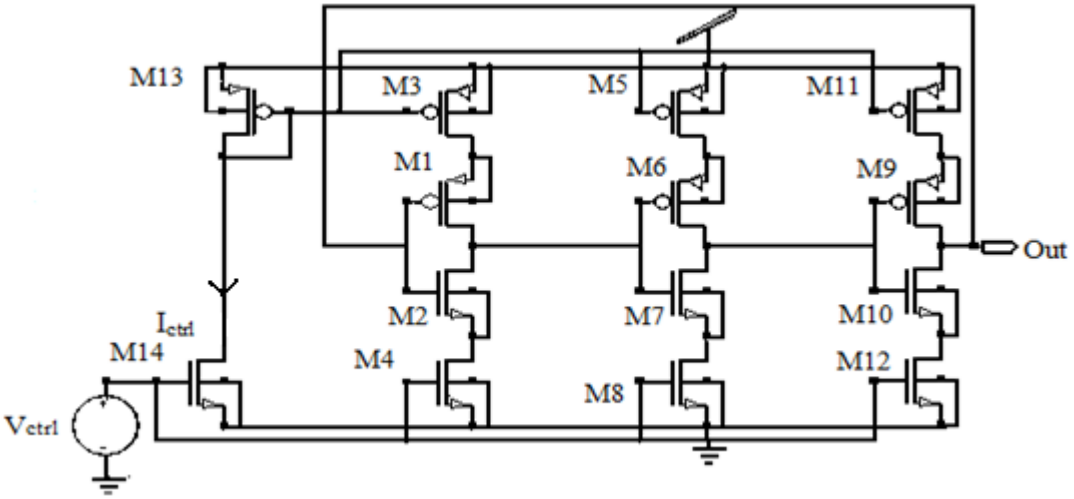
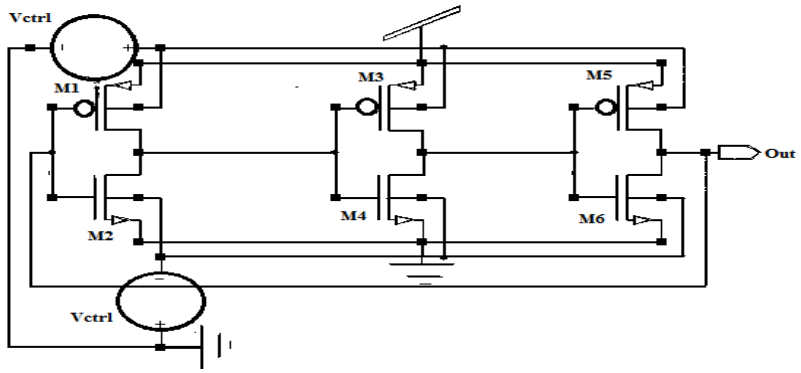
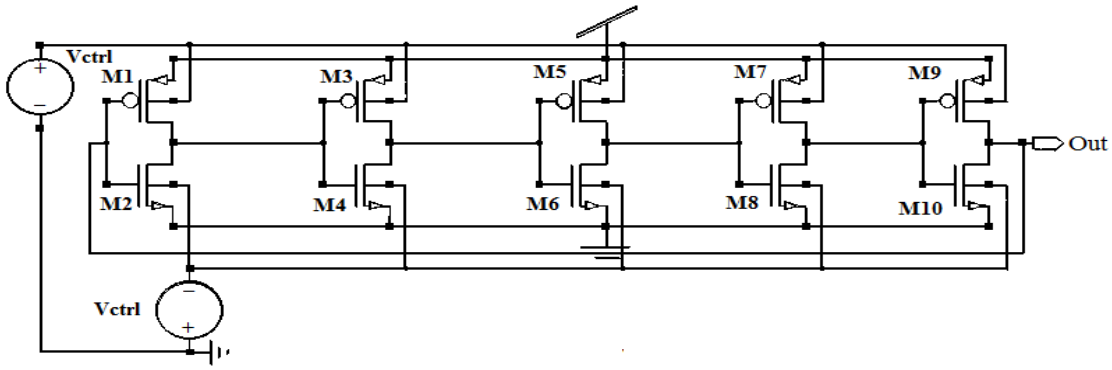


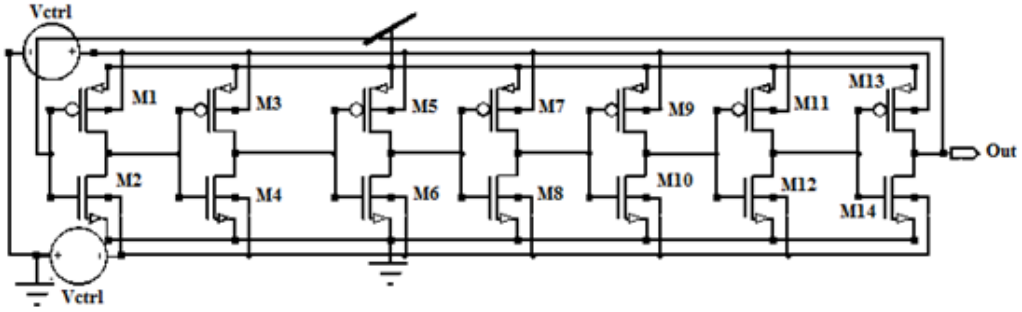
Figure 5. Schematic of Existing ring VCO (Current Starved VCO)



(a)



(b)



(c)

Figure 6. (a) (b) and (c) Proposed three, five and seven stage Ring VCO

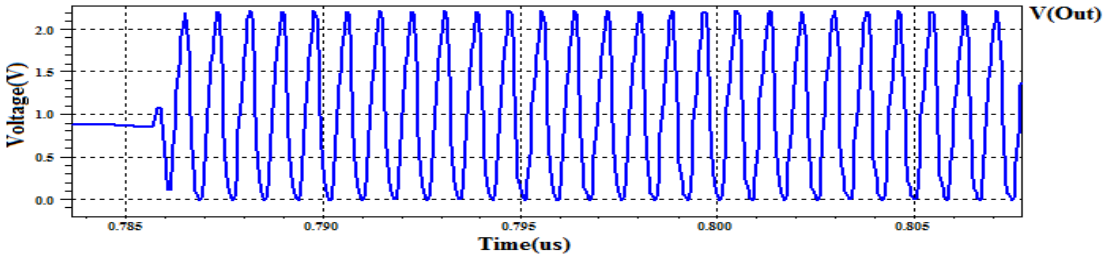


Figure 7. Output waveform of Existing three stage Ring VCO

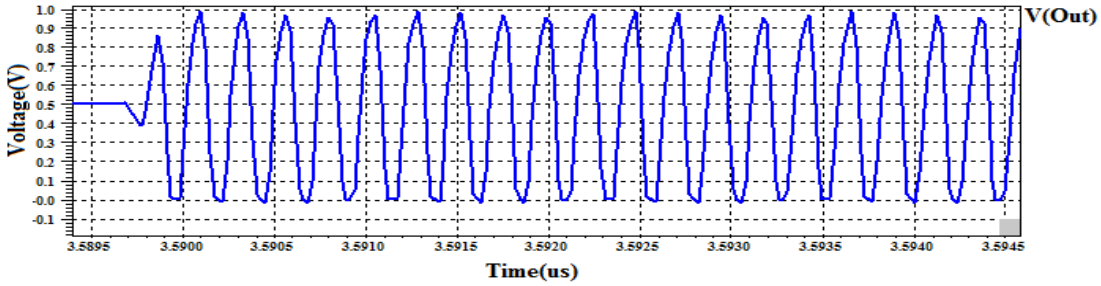


Figure 8. Output waveform of proposed three stage Ring VCO

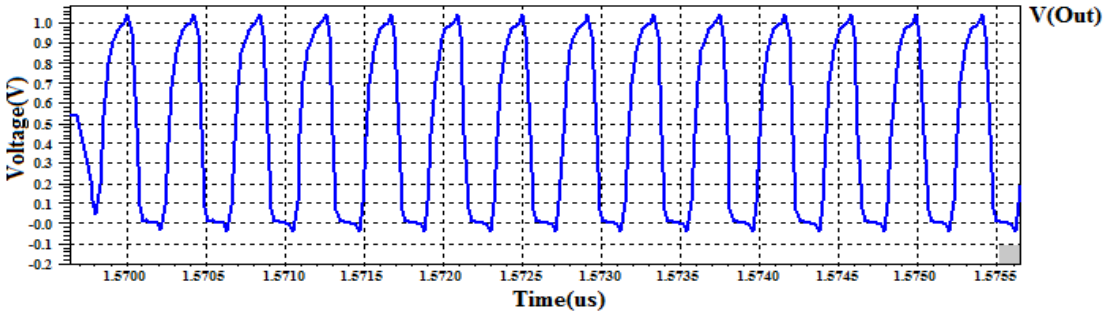


Figure 9. Output waveform of proposed five stage Ring VCO

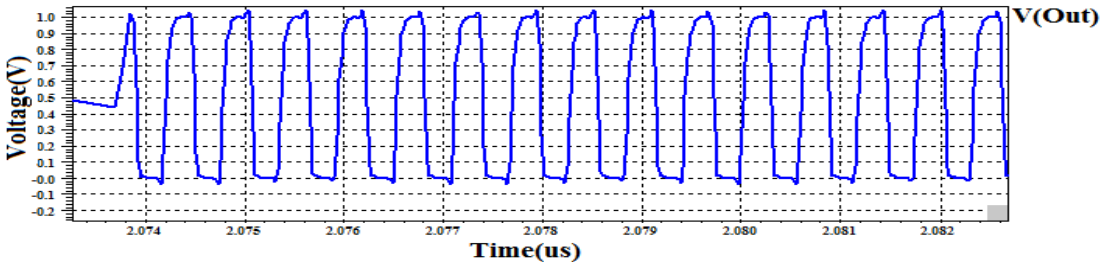


Figure 10. Output waveform of proposed seven stage Ring VCO

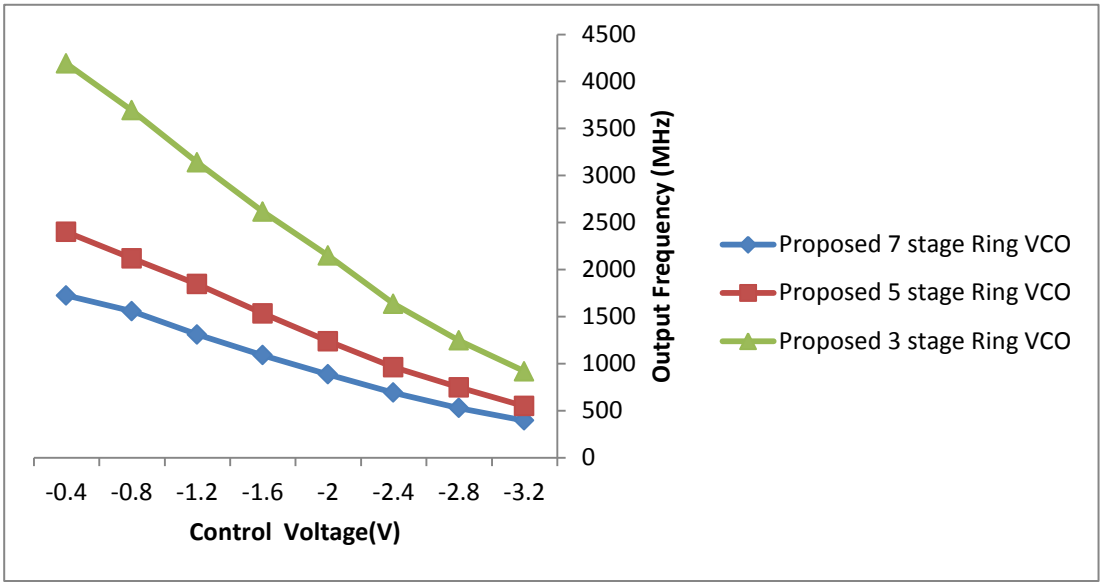


Figure 11. Output frequency variations with control voltage

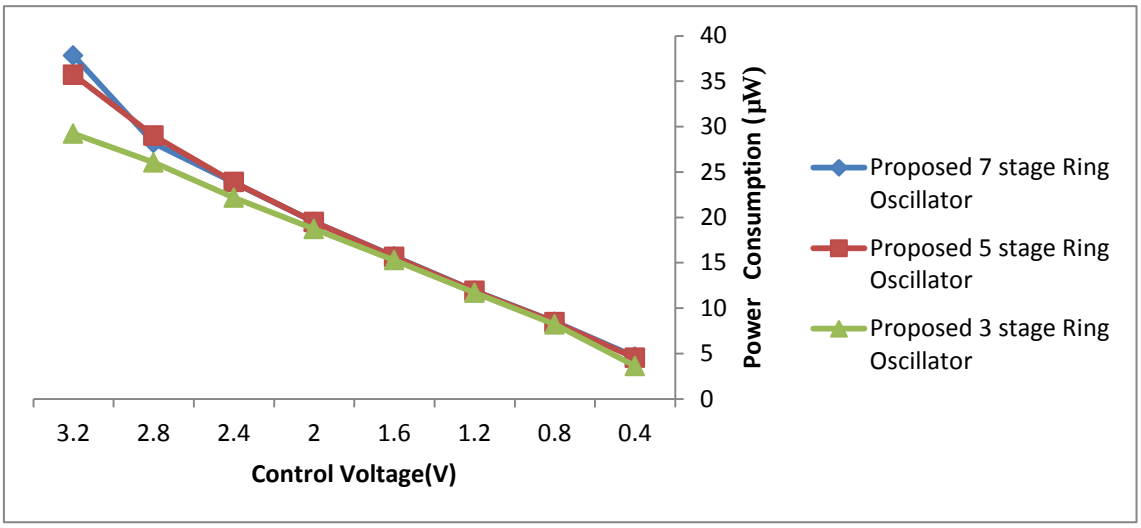


Figure 12. Power consumption variations with control voltage

Table I. Simulation results for Existing Ring VCO (Current Starved VCO)

Control Voltage(V)	Output Frequency (MHz)	Power Consumption (µW)
0.5	338.98	61.10
1.0	833.33	344.02
1.5	1108.00	399.29
2.0	1173.18	409.91
2.5	1203.39	413.75
3.0	1208.73	415.06

Table II. Simulation results for proposed three stage Ring VCO

Control Voltage(V)	Output Frequency (MHz)	Power Consumption (µW)
3.2	917.43	3.61
2.8	1245.90	8.20
2.4	1634.28	11.68
2.0	2147.02	15.26
1.6	2615.06	18.70
1.2	3138.04	22.16
0.8	3691.80	26.05
0.4	4189.53	29.21

Table III. Simulation results for proposed five stage Ring VCO

Control Voltage(V)	Output Frequency (MHz)	Power Consumption (µW)
3.2	546.44	4.51
2.8	746.26	8.44
2.4	961.53	11.88
2.0	1237.19	15.64
1.6	1532.05	19.49
1.2	1844.13	23.87
0.8	2118.77	28.98
0.4	2399.57	35.71

Table IV. Simulation results for Proposed seven stage Ring VCO

Control Voltage(V)	Output Frequency (MHz)	Power Consumption (µW)
3.2	393.70	4.64
2.8	526.31	8.48
2.4	689.65	11.90
2.0	884.95	15.68
1.6	1087.89	19.48
1.2	1308.21	23.83
0.8	1557.05	28.17
0.4	1723.60	37.82

Table V. Comparative analysis of Existing and Proposed Ring VCO

Parameters	Existing Ring VCO	Proposed Ring VCO
Output Frequency(MHz)	977.60	2447.38
Power Consumption(µW)	340.52	16.85
Bandwidth(MHz)	869.75	3272.10
No. of transistors	14	6
Supply Voltage(V)	3.0	1.0