

Design of Operational Transconductance Amplifier using Double Gate MOSFET

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Abstract

Operational Transconductance Amplifier is very popular in analog electronics industry due to its vast applications. Analog integrated circuits have been widely used for high frequency applications. OTA has number of applications like filters, analog multipliers and analog dividers. Double gate MOSFETs (DG-MOSFETs) are strong contenders for nano scale region due its better control over short channel effects. DG-MOSFET can be used in analog circuit applications as a four-terminal device. Back gate bias can be used for better tunability. The double gate based circuits provide additional gains in terms of area, power and speed. This paper presents double gate based OTA which has high gain over a wide bandwidth. The simulation results shows gain of 9.32 dB and bandwidth is 7GHz. The simulations are done using Tanner EDA Software Tool at 90nm technology.

Keywords: DG MOSFETs, OTA, Analog tunable circuits, Gain, Wide bandwidth, CMOS Process, Double gates, Self cascode technique

1. Introduction

Operational Transconductance Amplifier (OTA) is widely used in analog circuits. It is a voltage controlled current source open-loop amplifier, which is suitable for low-power and high speed circuits. Applications of operational amplifier are such as continuous time Gm-C filters, oscillators, and data converters. Recently, OTAs are developed in three trends -high frequency, high linearity and low power. At high frequencies, operational transconductance amplifiers (OTAs) are deemed to replace OPAMPs [S. Baswa, A. J. Lopez-Martin, J. Ramirez-Angulo, and R. G. Carvajal (2004)]. The ever increasing number of transistors that can be fabricated on a single chip has resulted decreased gate length. So we need design low power OTA. The supply voltage is reduced to achieve low power circuits. However, supply voltage reduction affects the voltage swing, the linearity and limits the bandwidth of the OTAs. The proposed double gate based OTA is the most suitable for low-voltage operation and large bandwidth. Depending on input and output, OTA can be categorized as:

- Single-input, single-output
- Differential-input-single output and
- Differential input- differential output

which is also called as fully differential OTA [E. Sanchez-Sinencio and J. Silva-Martinez (2000)]. The output current i_o for each type is given by following equations (1), (2), and (3), respectively:

$$i_o = -g_m v_i \quad [1]$$

$$i_o = g_m (v_{i+} - v_{i-}) \quad [2]$$

$$i_o = i_{o+} - i_{o-} = g_m (v_{i+} - v_{i-}) \quad [3]$$

where g_m is transconductance, v_{i+}, v_{i-} are differential inputs and i_{o+}, i_{o-} are differential output currents.

2. DG-MOSFETs device modeling and features

Nowadays, the silicon technology has strong affect on analog electronics industry due its large temperature tolerance. Electronics devices based on silicon are countless like – laptops, tablets, cellular, and many more. We

require low power and low voltage designing to compensate increasing number of devices on chip. With the introduction of 90 nm, silicon industry has moved to nano area to according to ITRS [International Technology Roadmap for Semiconductors (2001)]. There are number of problems due to scaling in conventional bulk CMOS device like SCE's, non-scaling of vertical dimensions [Y. Taur (1999)], [H.-S. P.Wong (2001)], [Yuan taur and Ning NH (2004)]. These problems degrade the performance of circuits and affect the reliability of devices. As number of devices increases on chip, the device gets heated and we require extra cooling or heat sinking system. We require the device circuit which work with low power dissipation, provide control SCE's, compensate increasing number of transistors on same chip and better energy storage for portable devices. Double gate devices have better control over SCE's and junction leakage due to improved electrostatic gate control of back gate [D. Jiménez, B. Iñiguez, J. Suñé and J. J. Saenz (2004)]. Double gate MOSFET is promising devices due to better scalability in nano circuits. DG-MOSFET exhibits an ideal 60 mV/dec subthreshold slope [D. J. Frank, S. E. Laux, and M. V. Fischetti,(1992)] and the threshold voltage of DG-MOSFET can be set by changing the work function of gate materials [H.S.P Wong, D. J. Frank, and P.M. Solomon (1998)], [Natzle, H.-J. Huang, J. Mezzapelle, A. Mocuta, S. Womack, M. Gribelyuk, E. C. Jones, R. J. Miller, H.-S. P.Wong,and W. Haensch (2002)]. The DG-MOSFET structure provides electrostatic coupling between conduction channel and gate electrode which allows additional gate length scaling by factor of 2 relative to the single gate MOSFET. The circuit symbols for n-type and p-type double gate MOSFETs are shown in Figure 1. With scaling down, the drain supply voltage V_{DD} and gate to source voltage V_{GS} also decreases.

It allows working in subthreshold region with increased transconductance g_m [M. V. R. Reddy, D. K. Sharma, M. B. Patil, & Rao(2005)]. They are also suitable for analog RF devices because of its ability to handle gigahertz frequency range. The double gates can work in two modes symmetrically driven double gate [SDDG] and independently driven double gate [IDDG] [M. Masahara et al (2005)]. The two device structures are shown in Figure 2. The front and back gates are connected to work in symmetrically driven mode and for analog tunable circuits, the front and back gates are biased at different voltages to achieve desired characteristics of device. The symmetrical driven mode is better than independently driven mode [Savas Kaya Hesham F. A. Hamed and Janusz A. Starzyk (2007), [MeiKei Jeong, H-S Philip Wong, Yuan Taur, Phil Oldiges, and David Frank (2000)].

3. Operational Transconductance Amplifier

The Figure 3 shows OTA based double gate MOSFETs. The reported OTA works in independently driven mode and shows very less gain [Ravindra Singh Kushwah , Shyam Akashe (2013)]. The input v_{in1} is given at front gates of transistors (M_1 and M_2) and v_{in2} is given at front gates of transistors (M_3 and M_4). The differential currents will flow and charge the load capacitor attached at output. This OTA can act as integrator. The biasing at back gates of transistors (M_1, M_2, M_3 and M_4) will be used for the tuning of circuit. We can use symmetric and asymmetric bias to shift the frequency response and change the trans-conductance. This OTA also acts as low pass filter of first order. We will design OTA to improve gain and bandwidth.

3.1 Small signal analysis of existing circuit

The given small signal circuit of Figure 3 is analyzed for output resistance and gain parameters. The circuit is symmetrical. The small signal equivalent is shown in Figure 4.

$$v_{in} = v_{gs1} = v_{gs2} = 0,$$

The output current i_o is given as

$$i_o = g_{m1}v_{gs1} + g_{m2}v_{gs2} + v_o(g_{ds1} + g_{ds2}) \quad [4]$$

which gives ratio of output voltage and output current as

$$\frac{v_o}{i_o} = \left(\frac{1}{g_{ds1} + g_{ds2}} \right) \quad [5]$$

The output resistance r_o is given as

$$r_o = r_{ds1} \parallel r_{ds2} \quad [6]$$

whereas r_{ds1}, r_{ds2} are resistances of M_1 and M_2 respectively. The transconductance g_m of existing OTA is:

$$g_m = g_{m1} + g_{m2} \quad [7]$$

whereas g_{m1} , g_{m2} are transconductances of M_1 and M_2 respectively. Finally the small signal gain A_o is

$$A_o = -g_m r_o \quad [8]$$

$$A_o = -g_m (r_{ds1} \parallel r_{ds2}) \quad [9]$$

4. Proposed OTA circuit

4.1 Circuit Description

Operational trans-conductance amplifiers (OTA) produce differential output currents, when differential input voltages are applied. The circuit diagram for proposed OTA is shown in Figure 5 which works in independently driven mode. The input v_{in1} is given at front gates of transistors M_1 , M_2 , M_3 , and M_4 and v_{in2} is given at front gates of transistors M_5 , M_6 , M_7 and M_8 . The input v_{in1} and biasing at back gate will drive transistors M_1 , M_2 to saturation region and transistors M_3 , M_4 to linear region. The input v_{in2} will drive (M_7 , M_8) to cutoff region and (M_5 , M_6) to linear region. The differential currents in both branches will flow and charge the load capacitor under consideration. This OTA can act as integrators because it drives a capacitive load. The self cascode OTA structure requires 8 transistors. In this circuit self cascode technique has been used which increases the output resistance and transconductance, thereby affecting the gain of circuit. As the input is provided to all transistors, it will increase transconductance. The use of the back gates allows the removal of the extra transistors which are required for transconductance tuning across the two branches of the OTA. This will save area as well as power.

We can tune this operational transconductance amplifier circuit using asymmetric bias ($v_{cn} \neq v_{cp}$) to shift the frequency response and change the transconductance. The OTA circuit serves as a low pass filter. The filter pass band extends up to gigahertz frequency range.

4.2 Small signal analysis

The proposed OTA circuit is symmetrical circuit, so it has same current in both branches. The equivalent small signal circuit is shown in Figure 6. The gain for proposed OTA is given by Equation 9, based on half circuit analysis.

For output resistance r_o , the input is set as

$$v_{in} = v_{gs1} = v_{gs2} = v_{gs3} = v_{gs4} = 0, \quad i_o = g_{m2}v_{gs2} + g_{m3}v_{gs3} + v_o(g_{ds2} + g_{ds3}) \quad [10]$$

Output resistance (r_o) is given by solving the ratio of output voltage and output current ($\frac{v_o}{i_o}$) as

$$\frac{v_o}{i_o} = \left(1 + \frac{g_{m2}}{g_{ds1}g_{sd2}}\right) \parallel \left(1 + \frac{g_{m3}}{g_{ds3}g_{sd4}}\right) \quad [11]$$

Considering $\left(1 \ll \frac{g_{m2}}{g_{ds1}g_{sd2}}\right), \left(1 \ll \frac{g_{m3}}{g_{ds3}g_{sd4}}\right)$

The above simplifies to output resistance (r_o) as

$$r_o = g_{m2}r_{ds1}r_{ds2} \parallel g_{m3}r_{ds3}r_{ds4} \quad [12]$$

As the input is given at the front gates of transistors M_1 , M_2 , M_3 and M_4 , so the equivalent transconductance g_m is observed as

$$g_m = g_{m1} + g_{m2} + g_{m3} + g_{m4} \quad [13]$$

The gain of the proposed OTA is defined in Equation 9, is given as

$$A_o = -g_m (g_{m2}r_{ds2}r_{ds1} \parallel g_{m3}r_{ds3}r_{ds4}) \quad [14]$$

Comparing the gain from Equation 9 and 14, the gain for proposed circuit is found high.

5. Simulation Results

The simulations of the proposed and the existing designs have been performed using Tanner EDA Tool version 13.0 and simulations are done on 90nm technology. In order to investigate that the proposed design has improved performance also the simulations are carried out for high gain, wide bandwidth. We also study here the effect of temperature on gain with increasing frequency.

5.1 Simulation results for n-type and p-type double-gate MOSFETs

The transfer characteristic of n-type and p-type double-gate MOSFETs are shown in Figure 7(a) and (b). The simulations are done for n-type and p-type double-gate MOSFETs as they are basic components which are used for designing proposed OTA circuit. The output drain current increases from -30 to 0 μA as input voltage changes from -0.5 V to $+0.5$ V for p-type and for n-type current increases from 0 to 15 μA as input voltage changes from 0 to 0.5 V. The current is a function of back gate biasing v_{bg} and front gate biasing v_{fg} .

5.2 Simulation results for DC analysis

A DC characteristic of existing circuit is shown in Figure 8(a) and (b). The output voltage is measured at different input voltage ranging from 0 to 1.5 V and is plotted from 0 to 1.5 V. The output voltage follows the input voltage linearly from range of 0.25 to 0.83 for existing circuit. The graph shows linear range of 580 mV.

A DC characteristic of proposed OTA is shown in Figure 9 (a) and (b). It is observed from the graph that the output is linearly following input over range of input voltage from 0.23 to 0.91 V. The linear range is 680 mV which is superior over the existing system. The increase in linear range is due to decreased overall capacitance of circuit.

5.3 Simulation results for AC analysis

The gain of existing circuit is 5.42 dB and bandwidth is 4.3 GHz observed as in Figure 10. The unity gain bandwidth is 6 GHz. The proposed circuit works at V_{DD} of 1.5 V. The control voltages are provided at back gates of transistors M_1 , M_2 and M_3 , M_4 is 0.28 and -0.94 respectively.

The AC response of the proposed OTA is shown in Figure 11. The gain of 9.32 dB is observed as compared to 5.42 dB of existing OTA. The gain is increased by using self cascode technique which also increases output resistance. The frequency at unity gain is 20 GHz which is higher than the existing OTA. The bandwidth is defined by the difference of lower and upper frequency at 3 dB down from maximum gain and is obtained as 7 GHz.

5.4 Simulation results for phase response

The phase responses for differential outputs of existing OTA are shown in Figure 12 (a) and (b). The phase margin from figure is measured as 56.33 degrees for existing circuit. Gain and phase margins are determined by finding the crossover points of the frequency response.

As a comparison, the phase responses of the proposed OTA are shown in Figure 13 (a) and (b). The phase margin for proposed OTA equals 94.6 degrees ($-85.4+180$).

5.5 Simulation results for studying the effects of temperature

The frequency response at different temperatures is shown in Figure 14. The temperature is varied from 0 to 100 degrees and gain is decreased from 10.63 to 5.63 dB. This behavior is easily explained on basis of transconductance being decreased with temperature. The decrease in gain is due to degradation in mobility of carriers at high temperature due to dominating phonon and surface scattering.

The overall comparison of different performance parameters of existing and proposed OTAs are made in Table I.

6. Conclusion

OTA performance is presented in this paper. This paper describes suitability of double gates for designing analog circuits. The proposed circuit offers wide unity gain bandwidth and high gain over existing OTA at given control voltage. The performance of proposed OTA has been compared with existing OTA and shows improved phase margin and linear range of operation.

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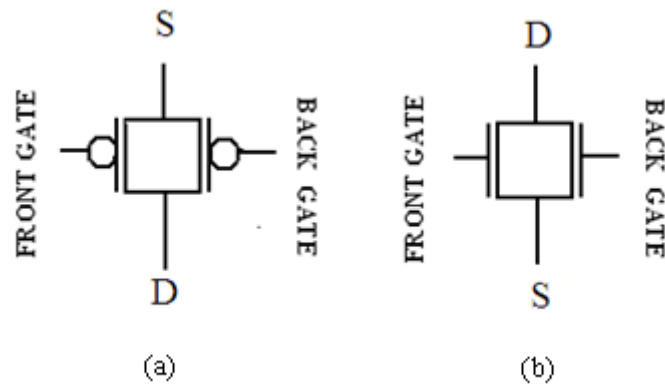


Figure 1. Circuit symbols for (a) p-type and (b) n-type double gate MOSFETs

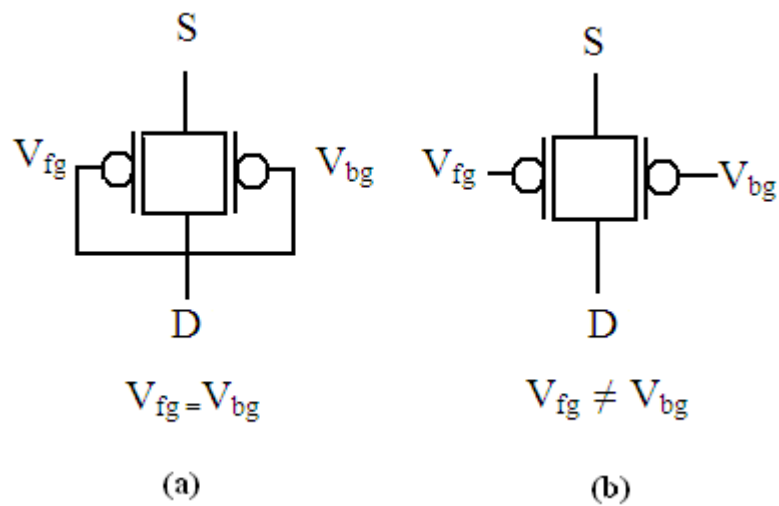


Figure 2. (a) and (b) Symmetrically and independently driven double-gate MOSFETs respectively

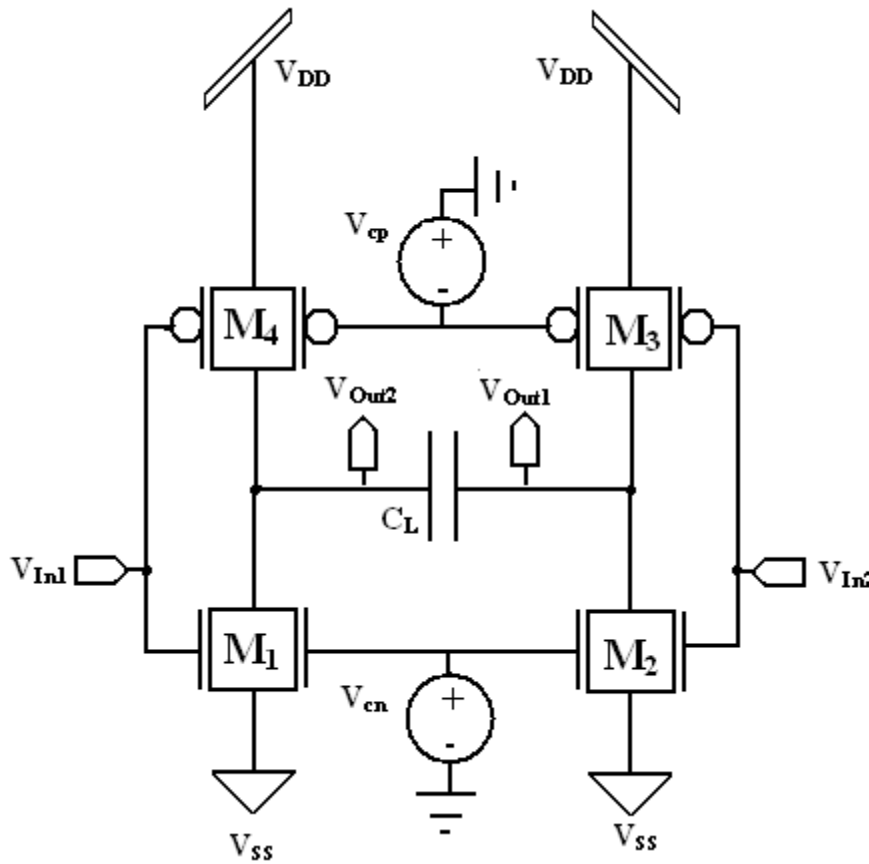


Figure 3. OTA based double gate MOSFETs

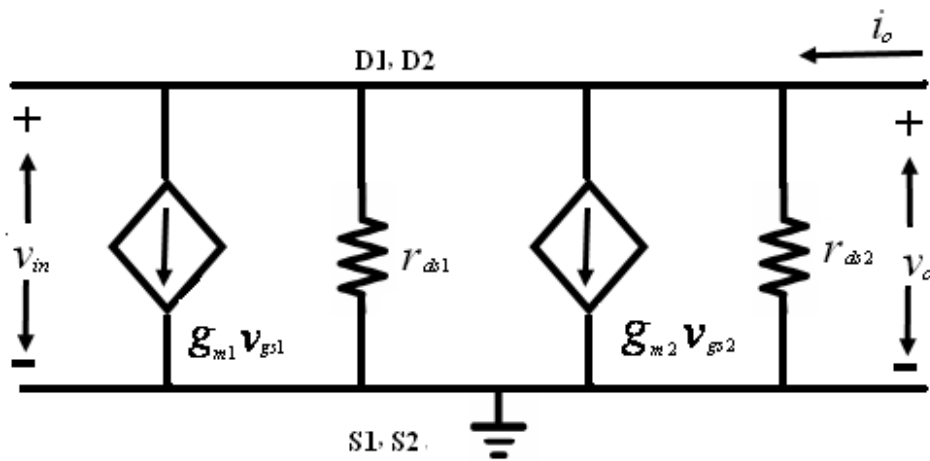


Figure 4. Small signal equivalent of existing circuit of Figure 3

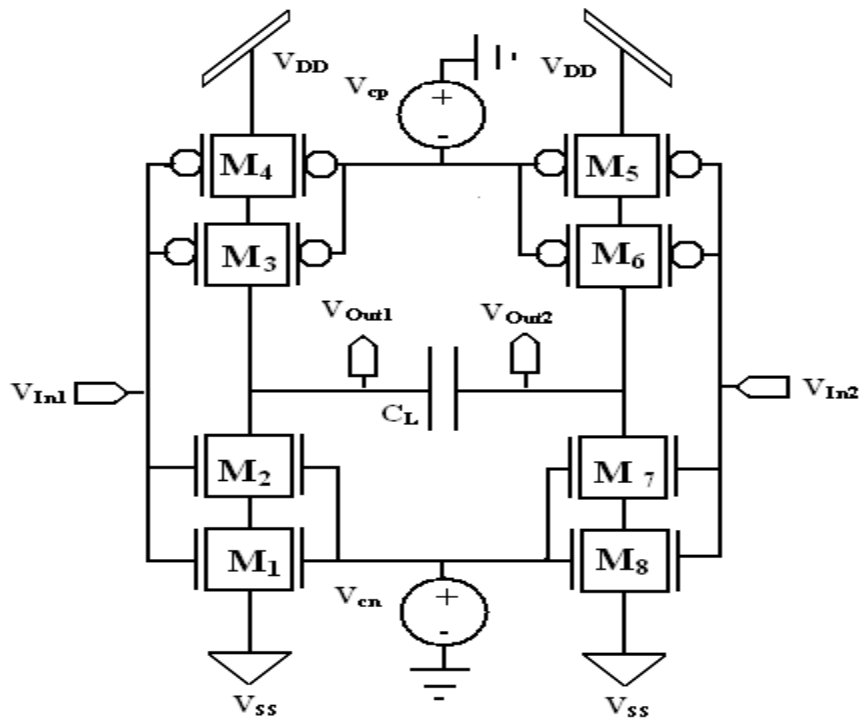


Figure 5. Proposed OTA circuit

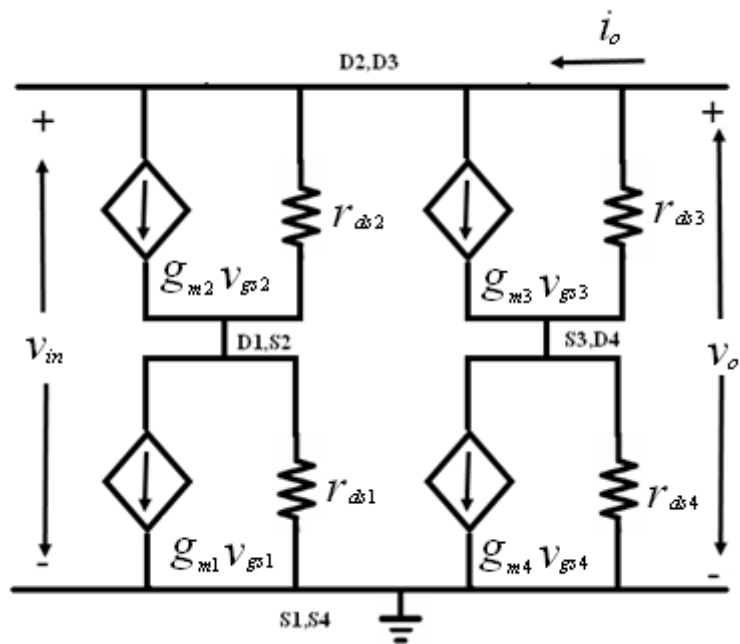
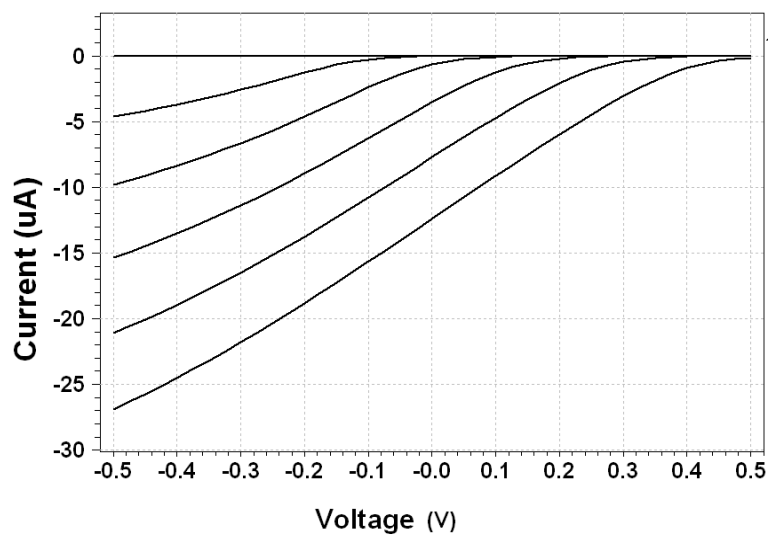
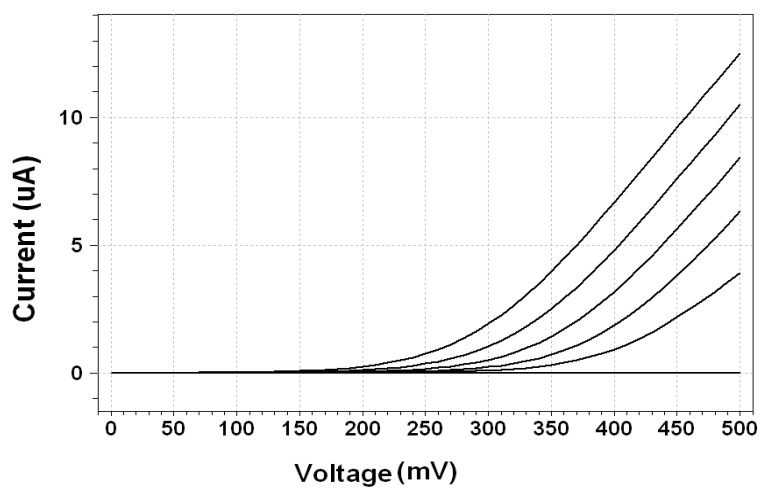


Figure 6. Small signal equivalent of circuit shown in Figure 5

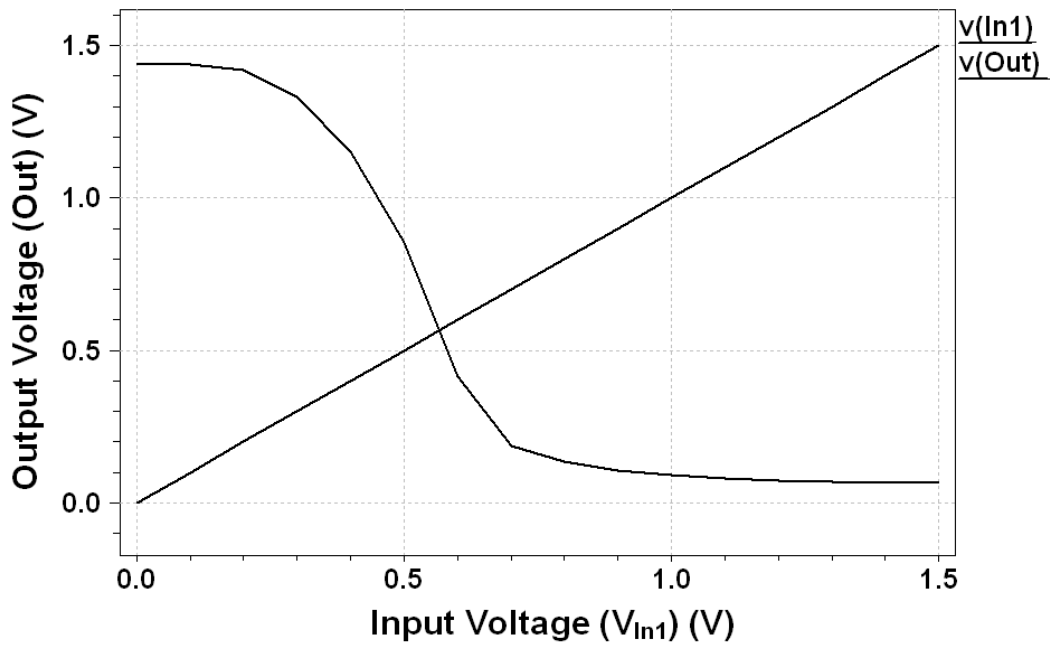


(a)

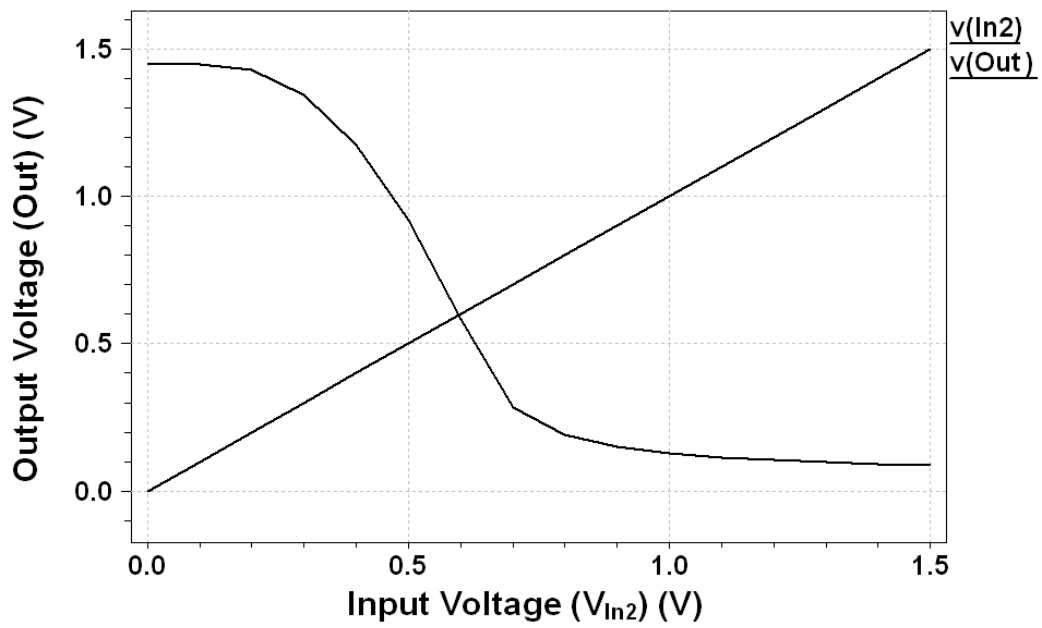


(b)

Figure 7. (a) and (b) Transfer characteristics of p-type and n-type D-G MOSFET respectively with back biasing

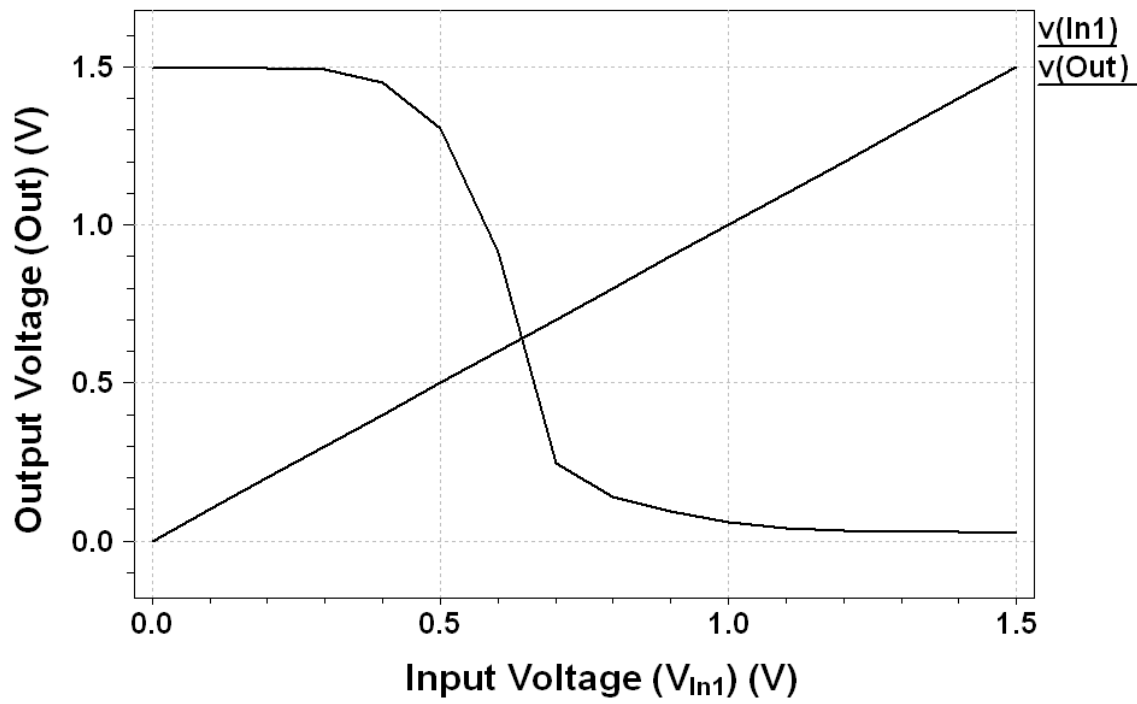


(a)

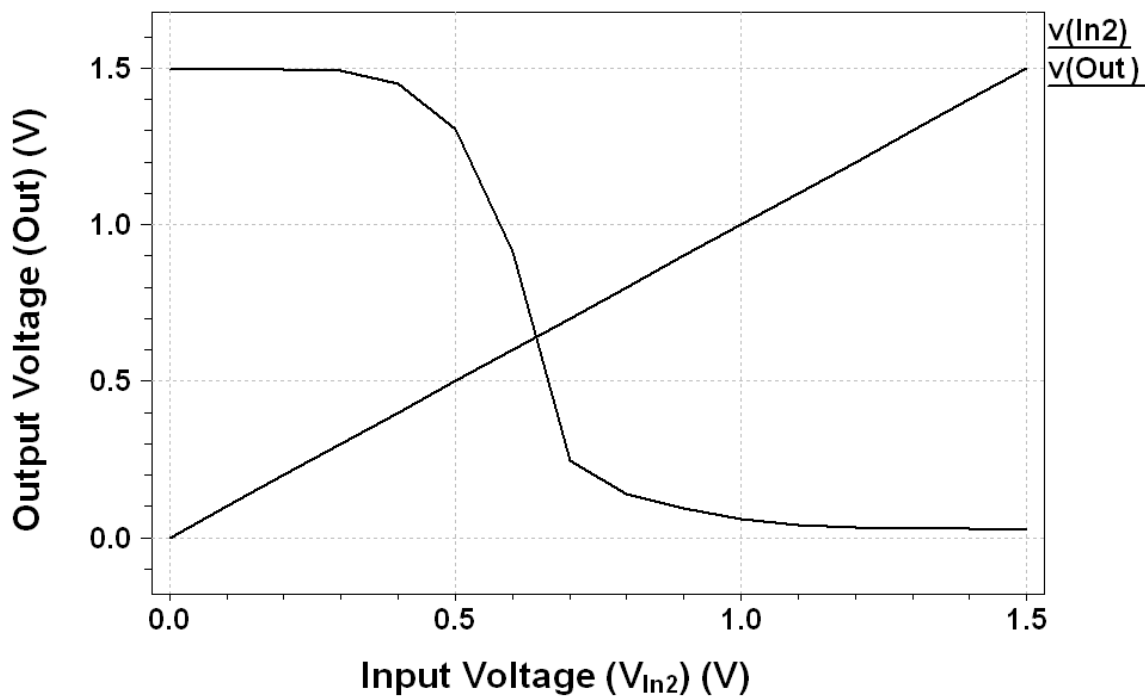


(b)

Figure 8. (a) and (b) DC characteristics of existing OTA for differential inputs and outputs respectively



(a)



(b)

Figure 9. (a) and (b) DC characteristics of proposed OTA for differential inputs and outputs respectively

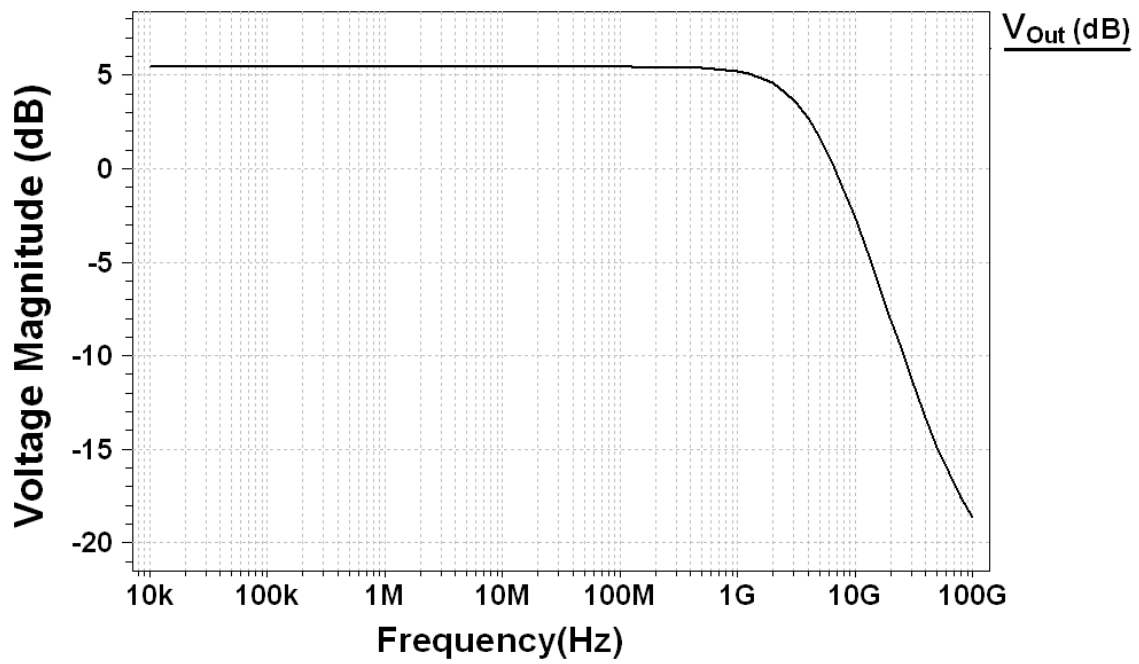


Figure 10. Differential gain of existing OTA

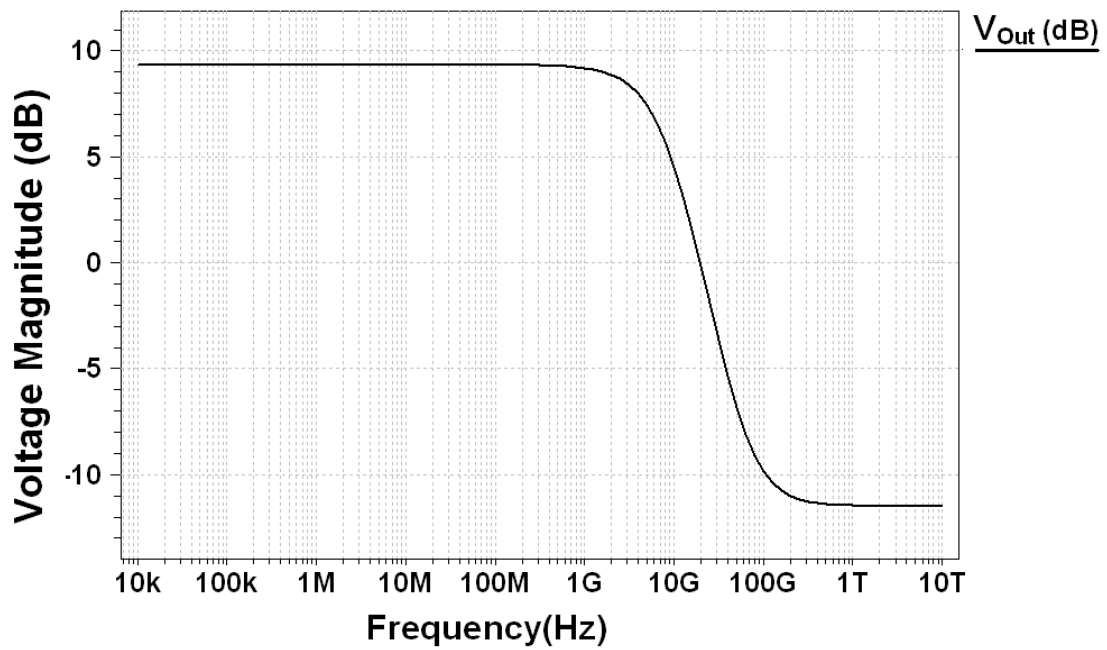


Figure 11. Differential gain of proposed OTA

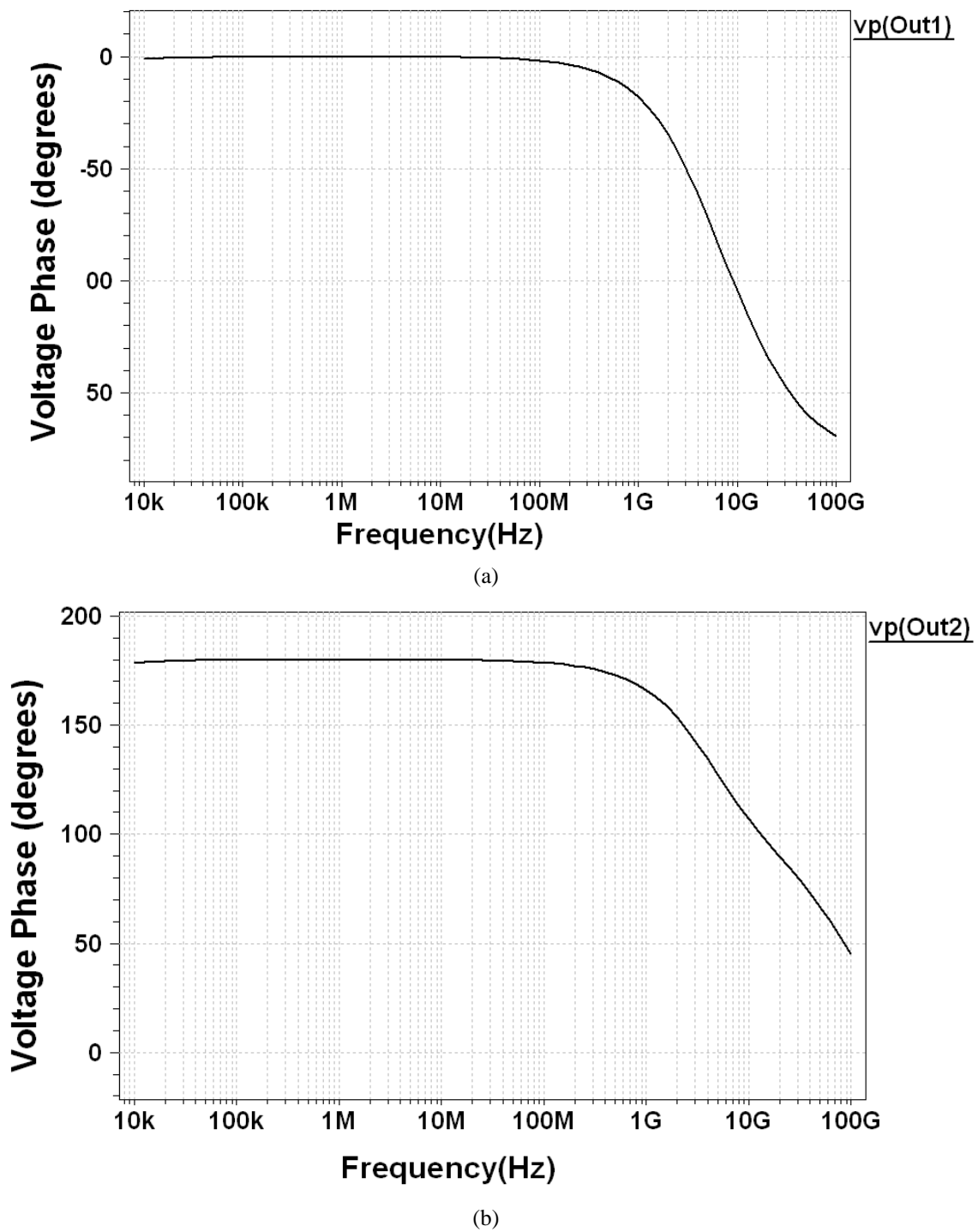
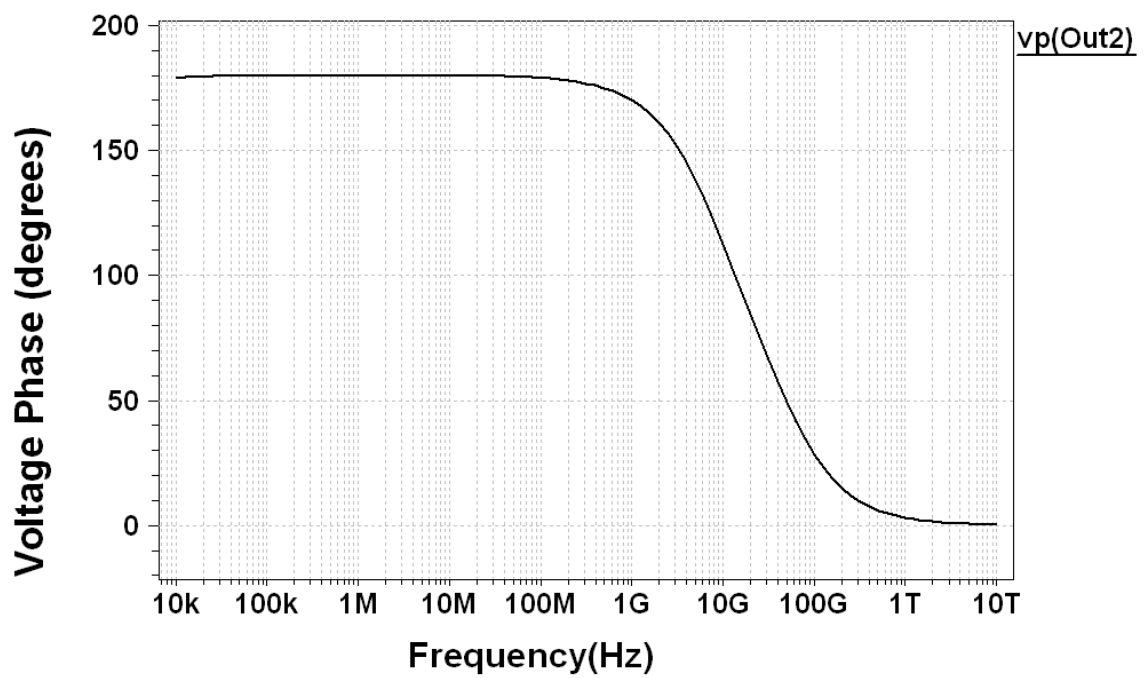
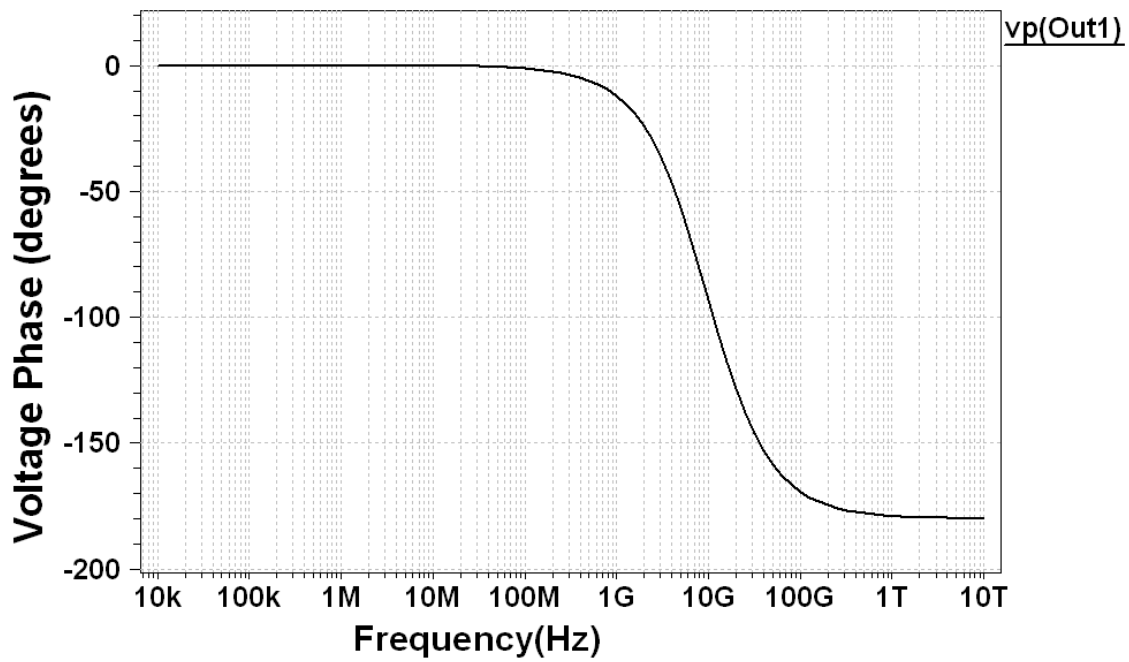


Figure 12(a) and (b) Phase response of existing OTA for differential outputs V_{out1} and V_{out2} respectively



(a)

(b)

Figure 13(a) and (b) Phase Response of proposed OTA for differential outputs V_{out1} and V_{out2} respectively

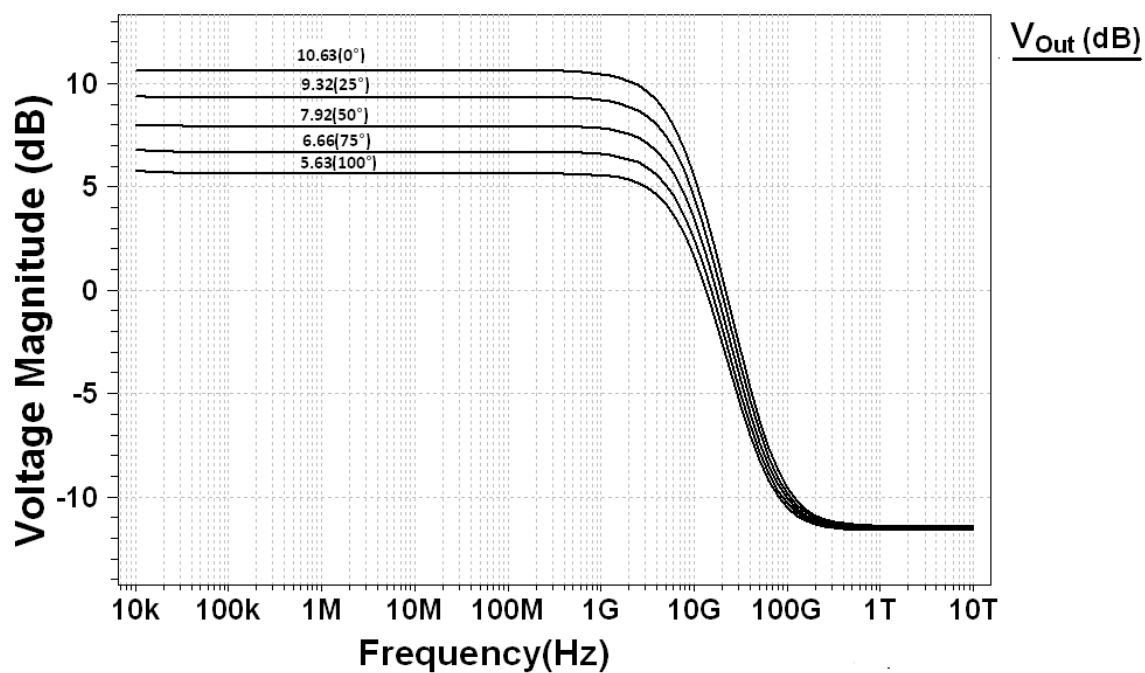


Figure 14. Effect of temperature on gain of proposed OTA

Table I. Comparison of different parameters for existing and proposed OTA

Parameters	Existing Circuit	Proposed Circuit
C_L (fF)	0.01	0.01
Gain (dB)	5.42	9.32
Bandwidth (GHz)	4.3	7
Unity Gain bandwidth(GHz)	6	20
Phase Margin(degrees)	56.3	94.6