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Area Efficient Level Sensitive Flip-Flops – A Performance Comparison

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Abstract

Due to increased demand of portable and battery operated devices, ultra-low power and high speed devices with less area requirement are important nowadays. Latch is the basic element for all the sequential circuits. This paper presents comparison of various circuits of D latch on the basis of power consumption, area efficiency and delay. Basically in these latches transmission gates are replaced by pass transistors to reduce the transistor count. Comparison results indicate that latch design with least transistor count is the best choice for portable applications.

Keywords: area efficient, latch, sub-threshold region, pass transistor, low power, level sensitive flip-flops, flip-flops.

1. Introduction

For long battery life and reliability of battery operated and portable applications, power consumption should be as low as possible [1]. Delay and area are also other parameters which should be reduced. Using less number of transistors leads to reduction in parasitic capacitances, chip area, propagation delay and power consumption [2][3]. Sub-threshold circuit operation is one way to reduce power consumption effectively because in sub-threshold region, all the transistors are operating with all the input and supply voltages less than threshold voltage (V_T).

Latches and flip-flops are basic sequential elements required for VLSI designs. Clocking networks are required to run these sequential elements. About 30%-70% of the total power of the system is consumed due to flip-flops and clocking network [4][5]. Therefore, to reduce the total power consumption [6][7] of any system, reduction in clock power and power associated with flip-flops and latches [8] is basic concern of VLSI designers.

In this paper different designs of latch are compared on the basis of power consumption, delay and area.

This paper is organized as follows: Section II describes the comparative analysis of different latches and section III draws the conclusion.

2. Comparative Analysis

2.1 10-Transistor (10T) Latch

10T latch [9] is used in memory applications. It is designed by using two transmission gates and three inverting gates as shown in Figure 1. Transmission gate acts like a contact which connects or breaks the path according to the control voltage. An inverter and a transmission gate form the feedback loop. Whenever the clock signal is active high then transmission gate at the input side becomes transparent and 'D' input is entered into the latch. This 'D' input is then passed through two inverters and output 'Q' is obtained which follows the input. Whenever clock signal is active low then transmission gate in the feedback path becomes transparent and output is fed back to the input and output is preserved. So this is a positive level sensitive flip-flop.

2.2 Conventional 8-Transistor (8T) Latch

This latch is designed by using two transmission gates and two inverters as shown in Figure 2 [10]. When clock signal, CLK is active high and CLKB signal, inverse of CLK signal, is active low, then transmission gate at input side allows the input data to enter the latch and this data signal is then passed through two inverters to provide the output Q. When clock signal, CLK, is active low and CLKB is active high, input transmission gate stops steering and another transmission gate, which is forming the feedback path, becomes transparent and output is fed back to the input [11]. Since, output follows the input when clock signal is active high, eight-transistor latch using transmission gates is positive level sensitive flip-flop.

2.3 8-Transistor (8T) Latch

8T latch [9] is designed by using pass transistors instead of transmission gates, therefore, two fewer transistors are required in this latch design as shown in Figure 3. NMOS_1 transistor forms the feedback loop. Whenever, clock signal is logic '0', then transistors PMOS_1 and PMOS_3 turn on and input 'D' is entered into the latch through transistor PMOS_1.

'D' signal is then passed through an inverter and PMOS_3. Finally output is obtained after passing through another inverter. When clock signal is logic '1', transistor NMOS_1 and NMOS_3 turn on and output is fed back through transistor NMOS_1, therefore output is preserved. This operation of the circuit confirms the static behavior of the latch. In the layout design of the conventional 8T latch, number of poly contacts is two and number of poly and metal overlap is only one as shown in Figure 4.

When clock signal is active high then intermediate signal is passed through NMOS_3 and when clock signal is active low then intermediate signal is passed through PMOS_3. Since nMOS is weak '1' device and pMOS is a weak '0' device, threshold loss problem occurs while using pass transistors. This phenomenon reduces the noise margin of the device. By using two inverters in the design, threshold loss problem is escaped. Since output changes at negative clock level and remains alike for positive clock level, therefore, 8T latch is negative level sensitive flip-flop.

8T latch is area efficient as compared to 10T latch design because two fewer transistors are used in 8T latch design. Both designs are simulated in sub-threshold region to observe power and delay at different temperatures, supply voltages and frequencies. Both designs are technology independent as they produce same results at 45nm and 65nm technologies.

As shown in Figure 5, Figure 6 and Figure 7, power consumption of 8T latch at various temperatures, supply voltages and frequencies is less as compared to 10T latch. Delay of 8T latch at various frequencies and supply voltages is also less as compared to that of 10T latch design as shown in Table 1 and Table 2. It is also observed through post layout simulations that the output resistance of 8T latch design is less and input resistance is large as compared to 10T latch design. From this point, it is clear that 8T latch design is better than 10T latch design in terms of power consumption, delay and area.

Now the conventional 8T latch is to be compared with the new design of 8-transistor latch. To operate circuit in sub-threshold region, it is required to keep the supply voltage always below the threshold voltage. At these supply voltages, delay introduced by the new design of 8T latch is comparatively very less as compared to that of the conventional one (Figure 8). For low power applications, devices work up to medium frequencies. The two designs are compared up to 1MHz frequency. Similar output is obtained when designs are compared at different temperatures in 45nm technology (Figure 9). Thus, new design of 8T latch is superior in performance than the conventional design.

2.4 7-Transistor (7T) Latch

The seven-transistor (7T) latch [10] is designed by using pass transistors instead of transmission gates (Figure 10). In this design clock distribution complexity is less because inverted clock signal is not required. Transistor M2 is used in feedback path. Whenever clock signal is active low, the pass transistor M1 turns on and the input data is passed through this transistor. After that, inverted output is passed to the input of the transistor M5. When clock signal is active high, pass transistors M2 and M5 turn on and the output 'Q' is obtained and output becomes constant as feedback loop is triggered. Layout of the 7T latch is made for post layout simulations (Figure 11). In layout design of the 7T latch, number of poly contacts is two and number of poly and metal overlap is only one.

Above mentioned new design of 8T latch and 7T latch are simulated in 45nm and 65nm and results in both of the technologies are analogous, so these designs are also technology independent.

These latch designs are operated in sub-threshold region. Average power consumption of both the latches is almost equal but delay introduced by 7T latch is tremendously less as compared to 8T latch as shown in Figure 12, Figure 13 and Figure 14, therefore power delay product (PDP) is also less.

As 7T latch design uses one transistor less than 8T latch design thus 7T latch design is area efficient also.

2.5 6-Transistor (6T) Latch

6T latch [12] also uses pass transistor logic [12]. This latch is formed by two pass transistors and two inverting

gates (Figure 11). PMOS transistor P1 is used to enter the input into the latch and NMOS transistor N1 is used for providing the feedback loop. Two inverters are used to overcome the problem of threshold loss caused by pass transistors.

When clock signal is active low, the pass transistor P1 becomes transparent and input data is passed through it (Figure 15). This input data is passed through two inverters to provide the output without any threshold loss. When clock signal is active high, then transistor N1 becomes active and output is fed back through it, therefore output remains constant. Layout of 6-transistor latch design is presented in Figure 16. In the layout design of the proposed 6T latch, number of poly contacts is two and there is no poly and metal overlap.

6T latch is also simulated and its results are compared with those of 7T latch. 6T latch is area efficient because one less transistor is used in its design as compared to 7T latch. These designs are compared in sub-threshold region.

As temperature increases, characteristics of the semiconductor device are also affected. It can be seen that the average power consumption of the designs increases with increase in temperature and power consumption of 6T design is remarkably lower than that of 7T design (Figure 17).

Circuits operating in sub-threshold region are very sensitive to the supply voltage. Sensitivity of the circuit towards the average power consumption increases with the decreasing power supply value. It can be seen that the power consumption of 6T design is lower than that of 7T design at different supply voltages (Figure 18).

Since in sub-threshold region, circuits work better up to medium frequencies, hence range of frequencies is taken from 50 kHz to 5MHz. The comparison of average power consumption with increasing operating frequencies is plotted and dominance of 6T design over 7T design in terms of average power consumption is indicated (Figure 19).

3. Conclusion

Low power consuming circuits are always first choice for any VLSI device construction. As the number of transistor decreases, performance of the design improves in terms of area, speed and power consumption. The simulation results, shown in conjunction with designs, indicate that the 6T design is much useful for low power devices and also it is area efficient. Thus for systems where low power consumption and area are of primary interest within a certain power budget, 6T is a better choice.

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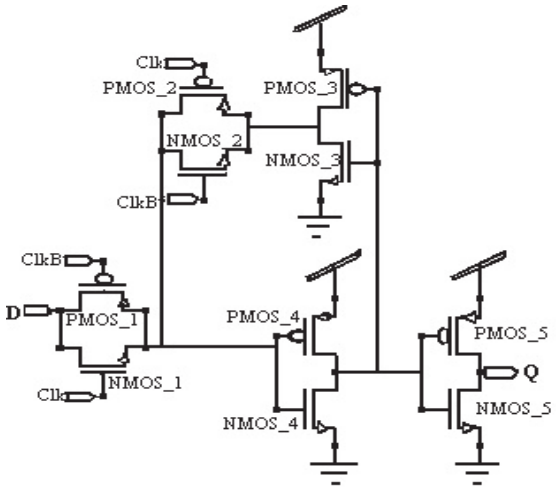


Figure 1. 10-Transistor Latch

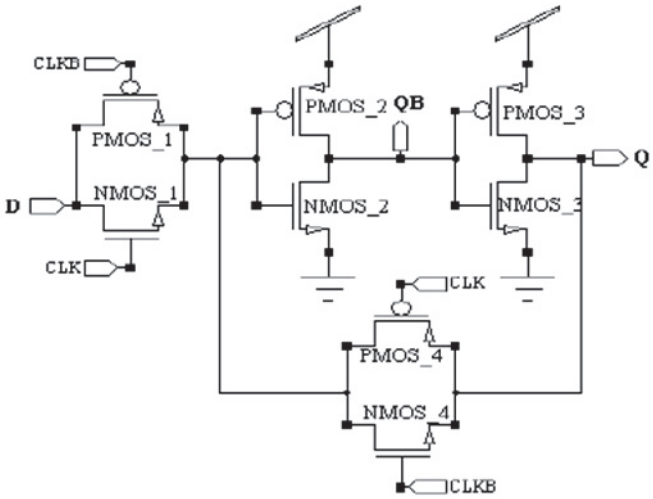


Figure 2. Conventional 8-Transistor Latch using Transmission Gates

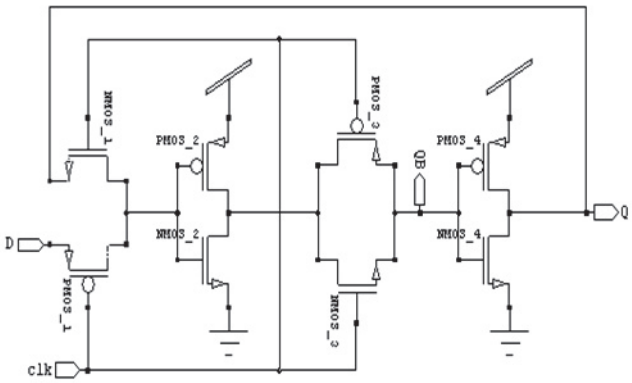


Figure 3. 8-Transistors Latch

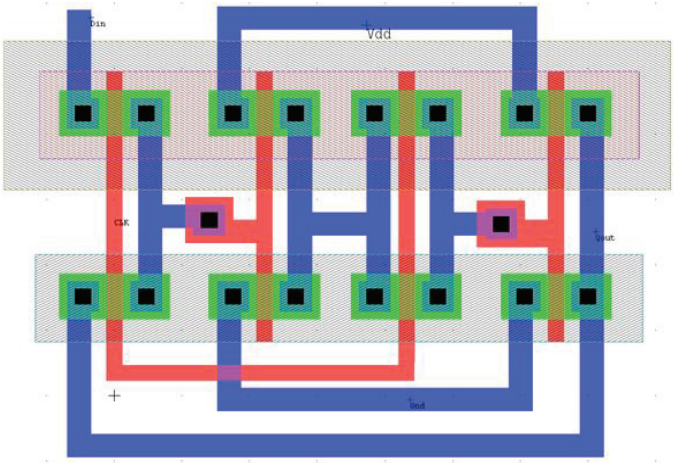
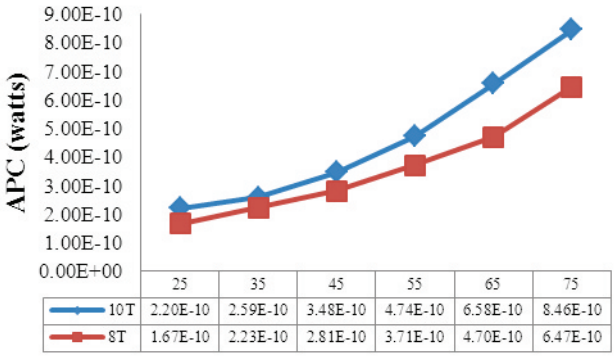
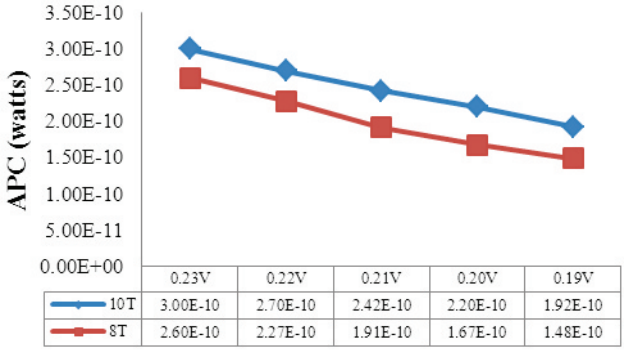


Figure 4. Layout Design of 8T Latch



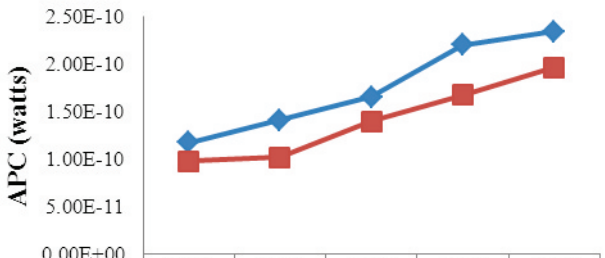
	25	35	45	55	65	75
10T	2.20E-10	2.59E-10	3.48E-10	4.74E-10	6.58E-10	8.46E-10
8T	1.67E-10	2.23E-10	2.81E-10	3.71E-10	4.70E-10	6.47E-10

Figure 5. Average Power Consumption at Various Temperatures (^{O}C) in 45nm Technology



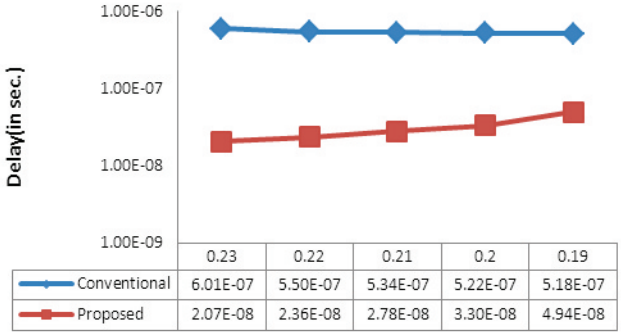
	0.23V	0.22V	0.21V	0.20V	0.19V
10T	3.00E-10	2.70E-10	2.42E-10	2.20E-10	1.92E-10
8T	2.60E-10	2.27E-10	1.91E-10	1.67E-10	1.48E-10

Figure 6. Average Power Consumption at Various Supply Voltages in 45nm Technology



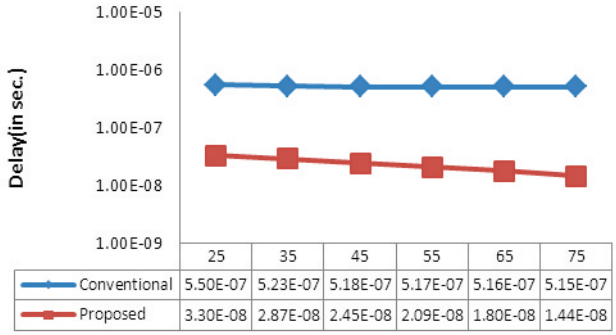
	50kHz	100kHz	500kHz	1MHz	5MHz
10T	1.17E-10	1.41E-10	1.65E-10	2.20E-10	2.35E-10
8T	9.77E-11	1.02E-10	1.40E-10	1.67E-10	1.97E-10

Figure 7. Average Power Consumption at Various Frequencies in 45nm Technology



	0.23	0.22	0.21	0.2	0.19
Conventional	6.01E-07	5.50E-07	5.34E-07	5.22E-07	5.18E-07
Proposed	2.07E-08	2.36E-08	2.78E-08	3.30E-08	4.94E-08

Figure 8. Delay at Various Voltages in 45nm Technology



	25	35	45	55	65	75
Conventional	5.50E-07	5.23E-07	5.18E-07	5.17E-07	5.16E-07	5.15E-07
Proposed	3.30E-08	2.87E-08	2.45E-08	2.09E-08	1.80E-08	1.44E-08

Figure 9. Delay at Various Temperatures (^{O}C) in 45nm Technology

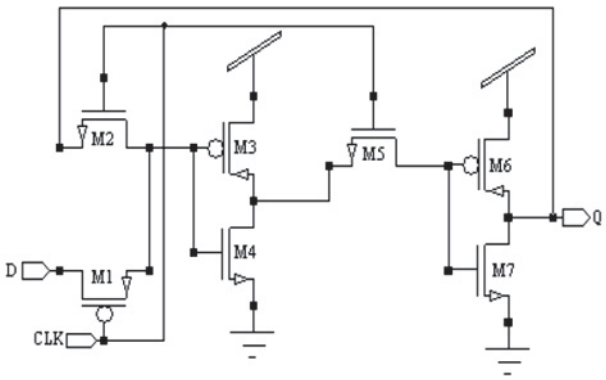


Figure 10. Seven-Transistors Latch

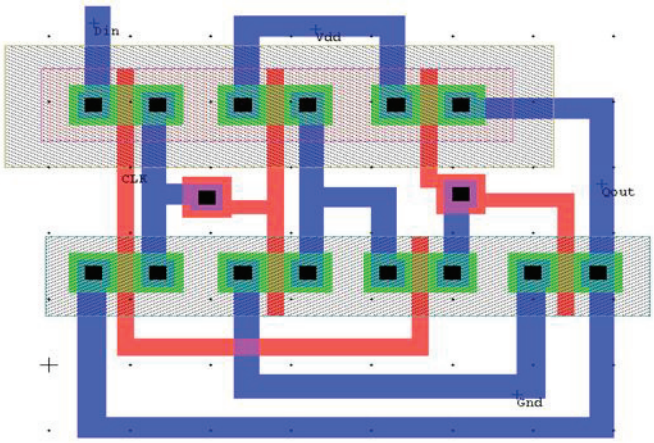


Figure 11. Layout Design of Proposed 7T Latch

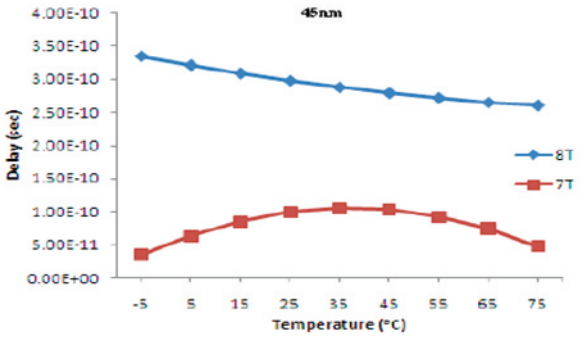


Figure 12. Delay at Various Temperatures (^{O}C) in 45nm Technology

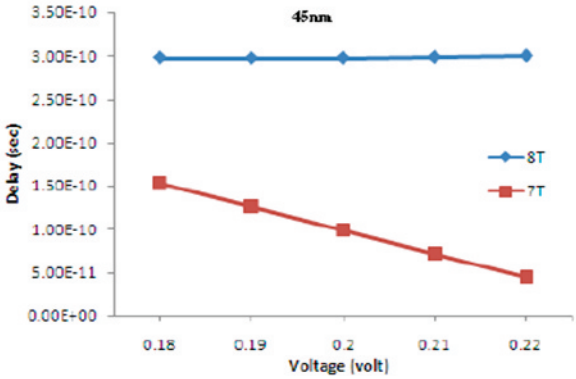


Figure 13. Delay at Various Supply Voltages in 45nm Technology

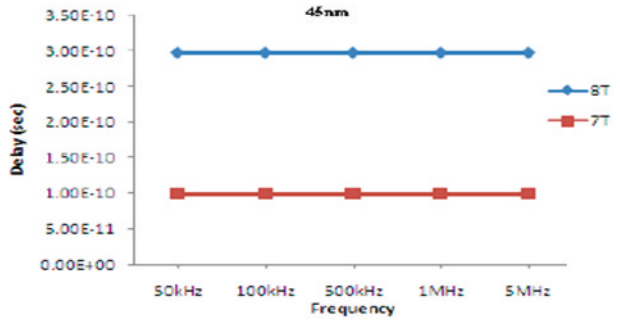


Figure 14. Delay at Various Frequencies in 45nm Technology

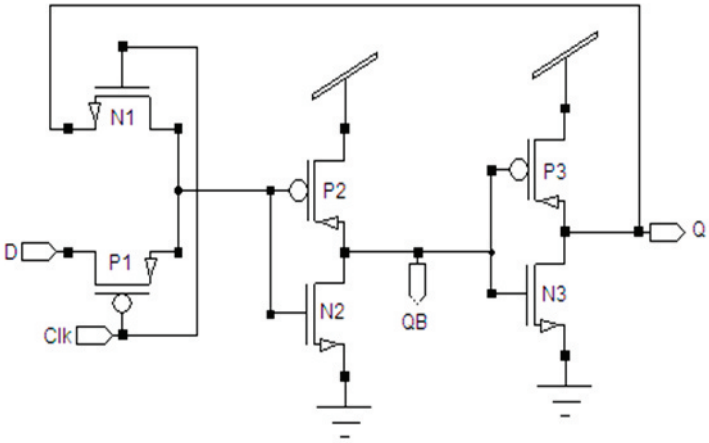


Figure 15. Six-Transistor Latch

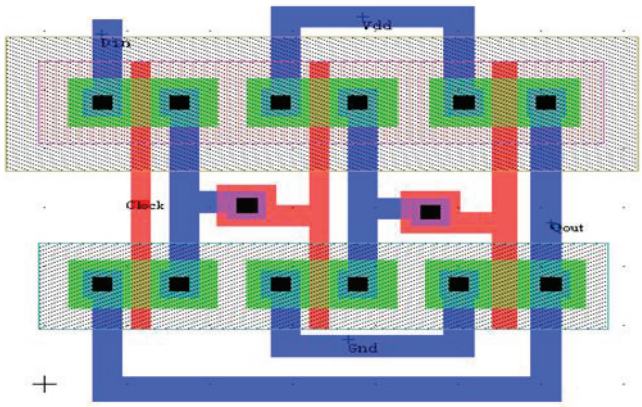


Figure 16. Layout Design of 6T Latch

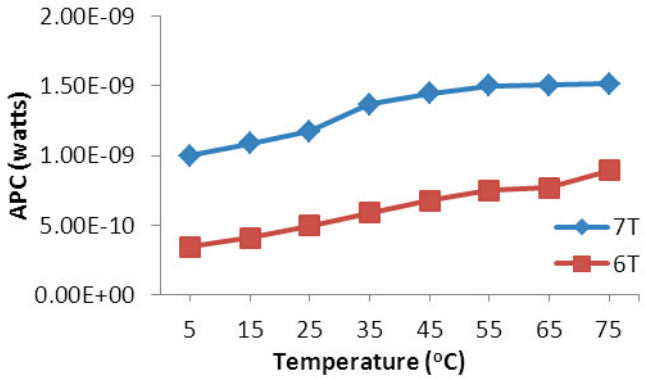


Figure 17. Average Power Consumption at Various Temperatures (^{O}C) in 65nm Technology

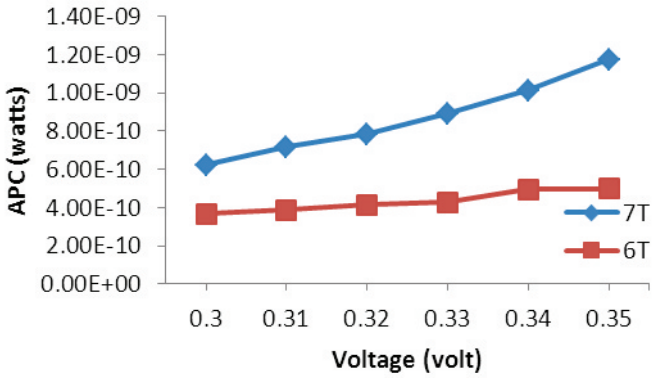


Figure 18. Average Power Consumption at Various Supply Voltage in 65nm Technology

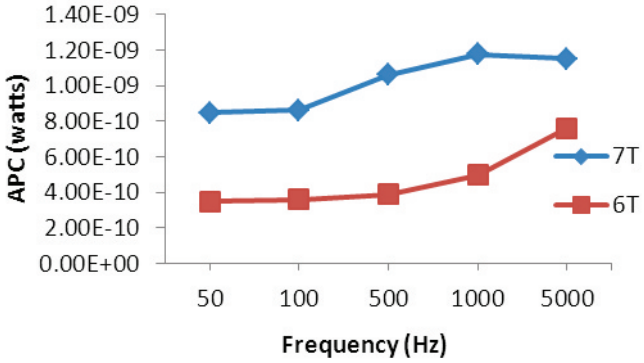


Figure 19. Average Power Consumption at Various Frequencies in 65nm Technology

Table 1. Delay (in sec.) at Various Temperatures (^{O}C) in 45nm Technology

Temperature (^{o}C)	10T	8T
25	5.5553e-007	3.2987e-008
35	5.2888e-007	2.8724e-008
45	5.1818e-007	2.4455e-008
55	5.1704e-007	2.0920e-008
65	5.1646e-007	1.8026e-008
75	5.1479e-007	1.4421e-008

Table 2. Delay (in sec.) at Various Supply Voltages (Volts) in 45nm Technology

Supply Voltage	10T	8T
0.23V	5.1892e-007	2.0715e-008
0.22V	5.2894e-007	2.3595e-008
0.21V	5.4441e-007	2.7832e-008
0.20V	5.5553e-007	3.2987e-008
0.19V	5.0102e-007	4.9428e-008

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