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Design of Second Order Low Pass and High Pass Filter using Double Gate MOSFET based OTA

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Abstract

OTA-C filters are one of the most widely used as continuous time filters. It is because they are fast active integrators, provides low-power operation and tuning of the filter characteristics at higher frequencies. At high frequencies, the OP AMP based active filters has limited performance. We cannot change the values of resistors and inductors but OTA-C filter provides ability to change their values by changing the transconductance of OTA. Second order low and high pass filter structures have widespread applications. The double gate MOSFETs show better performance in the nanometer range of operation. Because it has better control over short channel effects (SCE's) and other scaling related problems like gate leakage, sub-threshold conduction. Double gate MOSFET is four terminal device and back gate can be used for biasing which can tune the characteristics of circuit. This will provide additional advantage of low power and reduced area. This paper presents second order low pass and high pass filter based on double gate OTA for VHF and UHF frequency applications. The proposed filter consists of two OTAs and two capacitors. This filter shows low sensitivity to passive components, low component count and ease in design. The simulation results shows pass band frequency of 14MHz and power consumption of 153.4 µwatt. The simulations are done using Tanner EDA version 13.0 at 90nm technology.

Keywords: DG MOSFETs; OTA-C; Analog tunable circuits; Gain; Bandwidth; Double gate; Self cascode technique; Low pass filter; High pass filter.

1. Introduction

Analog filters play a very significant role in every electronic system. The designing of filter using passive ladder filter as a prototype for active filters, such as operational transconductance amplifiers and capacitors (OTA-C), has become very popular. There is a growing interest in continuous time filters because of applications such as portable electronic equipment, wireless receivers, continuous-time analog-to-digital converters and etc. The block diagram of filter is shown in Figure 1. The OTA-C filters have several advantages over the more typical operational amplifier configurations. These advantages are such as electronic filter tuning, high frequency of operation and fully integrated filter design [E. Sánchez-Sinencio, E., R. L. Geiger, and H. Nevarez-Lozano(1988)],[Silva-Martinez, J. Silva-Martinez(2001)]. In OTA-C filters, tuning of filter can be achieved by changing the parameter transconductance of an OTA. The filter performance depends upon the properties of its constituent components i.e. OTA and capacitors. Since transconductance of the filter is proportional to current or voltage bias level, frequency response can be changed by modifying the bias level of the OTA.

The remaining paper is organized in five sections:

Section 2 describes the architecture of filter and transistor level implementation of OTA is given in Section 3. Section 4 gives information about proposed filter. Section 5 shows simulation results and finally section 6 concludes the paper.

2. Filter architecture

Filters using OTAs and capacitors are called OTA-C filters or Gm-C filters. The block diagram of OTA is shown in Figure 2. An OTA integrator is the simplest OTA-C filter, which can be called as a first order low pass filter. It consists of only OTA and a capacitor. For designing of OTA-C filter, the passive ladder is taken as prototype and then using signal flow graph, and finally the required filter circuit is designed. The higher order filter can be designed to improve the frequency response and increase the sharpness of filter. They can be designed using different topologies like- cascade and passive ladder. The different types of filters like band pass, high pass and band reject filter can be realized using OTA and capacitor [E. Sanchez-Sinencio and J. Silva-Martinez(2000)],[B. Razavi(2000)].

3. Circuit implementation

3.1. Operational transconductance amplifier based on double gate MOSFET

Operational transconductance amplifiers (OTA) are most preferred active element because its transconductance can be controlled electronically by adjusting the bias current. It is a voltage controlled current source open-loop amplifier, which is suitable for low-power and high speed circuits. OTA are designed using different technologies such as bipolar, CMOS, bi-CMOS, to improve the performance of circuit. We require the device circuit which work with low dissipation, provide control SCE's and better energy storage for portable devices. Double Gate devices have better control over SCE's and junction leakage due to improved electrostatic gate control of back gate[Semiconductor Industry Association (SIA)(20001)],[H.-S. P.Wong (2001)],[M. Masahara et al (2005)]. The proposed OTA is based on independent driven double gate MOSFET. In independent mode, the different biasing is given at both gates, thus the new functions can be provided to improve the operation of circuits by exploiting the threshold voltage coupling between the two gates. The back gate is used provide biasing which tunes the circuit. Consequently, it is possible to design high-performance and low-voltage mixed-signal systems using DG-MOSFET devices with added gain of tunable analog characteristics as well as reconfigurable logic functionality.

3.2 Circuit description of OTA

Operational trans-conductance amplifiers (OTA) produce differential output currents, when differential input voltages are applied. The proposed OTA works in independently driven mode as shown in Figure 3 [Jagdeep Kaur Sahani, Shruti Suman, P. K. Ghosh (2014)]. The input v_{In1} is given at front gates of transistors (M_1, M_2, M_3, and M_4) and v_{In2} is given at front gates of transistors (M_5, M_6, M_7 and M_8) .The input v_{In1} and biasing at back gate will drive (M_1, M_2) to saturation and (M_3, M_4) to linear region. The input v_{In2} will drive (M_7, M_8) to cutoff region and (M_5, M_6) to linear region. The differential currents in both branches will flow and charge the load capacitor under consideration. This OTA can act as integrator because it drives a capacitive load. The self cascode OTA structure requires 8 transistors. In this circuit self -cascode technique has been used which increases the output resistance and transconductance, thereby effecting the gain of circuit. As the input is provided to all transistors, it will increase transconductance. The use of the back gates allows the removal of the extra transistors which are required for trans-conductance tuning across the two branches of the OTA. This will save area as well power. We can tune this operational trans-conductance amplifier circuit using asymmetric bias $(v_{cn} \neq v_{cp})$ to shift the frequency response and change the trans-conductance. The OTA circuit serves as a low pass filter. The filter pass band extends up to gigahertz frequency range.

3.3 High frequency model of OTA

The OTA circuit is symmetrical circuit, so it has same current in both branches. The equivalent high frequency small signal model of circuit is shown in Figure 4. As the input is given at the front gates of transistor M_1, M_2, M_3 and M_4, so the equivalent transconductance g_m is observed as:

$$g_m = g_{m1} + g_{m2} + g_{m3} + g_{m4} \qquad [1]$$

The effective transconductance is increased which will improves the frequency response of proposed filter. The cascode structure removes the miller effect by providing isolation between input and output which will increase bandwidth, unity gain bandwidth and improves phase margin of OTA [Sedra Smith (2001)]. The given model has two poles. The -3dB frequency is given by dominant pole at node Y and next first non- dominant pole is seen at node X. The effect of pole at node Z is included in output node and frequency of dominant pole is given by equation 2:

$$w_{p1} = \frac{1}{[g_{m3} r_{o3} r_{o4} (C_L + C_2) + r_{o4} C_3] s + 1} \qquad [2]$$

$$w_{p2} = \frac{g_{m2}}{C_1} \qquad [3]$$

The cascode structure provides high bandwidth as given by w_{p1}. The non- dominant pole w_{p2} at high frequency is given by equation 3 which provides high unity gain bandwidth owing to increased transconductance of OTA structure. This circuit avoids additional poles which improves stability and phase margin.

4. Filter design

OTA based on double gate MOSFET is very suitable for implementing second order filter [O. Naess and Y. Berg (2000)]. The wide bandwidth and increased transconductance property of OTA is used to design filter. Figure 5 illustrates a second-order OTA-C low pass and high pass filter consisting of two OTA of transconductance (g_{m1} and g_{m2}) and two capacitors (C_1 and C_2). The signal graph shows the direction of current in filter design. The signal flow graph of the given low and high pass filter is shown in Figure 6.

The equivalent passive component implementation of low pass filter is given in Figure 7. The OTA1 and OTA2 forms along with capacitor forms inductor L the equivalent inductance is given by equation 4.

$$L = \frac{C_1}{g_{m1} g_{m2}} \qquad [4]$$

where g_{m1}, g_{m2} are the transconductances of OTA1 and OTA2. OTA2 acts as resistor of resistance value as follows:

$$R = -\frac{1}{g_{m2}} \qquad [5]$$

The equivalent resistance is given by inverse of transconductance. The transfer function for low pass filter is given by equation 6.Using voltage divider rule in circuit given in Figure 7, the input and output is given as:

$$\frac{V_{lp}}{V_{In1}} = \frac{Z_2}{Z_1 + Z_2} \qquad [6]$$

where $Z_2 = \dfrac{R\dfrac{1}{sC_2}}{R + \dfrac{1}{sC_2}}$ and $Z_1 = sL$.substituting values of Z_1 and Z_2 gives following equation 7:

$$\frac{V_{lp}}{V_{In}} = \frac{\dfrac{1}{LC_2}}{s^2 + s\dfrac{1}{RC_2} + \dfrac{1}{LC_2}} \qquad [7]$$

Putting the values of L and R , the transfer function reduces to:

$$\frac{V_{lp}}{V_{In1}} = \frac{g_{m1} g_{m2}}{s^2 C_1 C_2 + sC_1 g_{m2} + g_{m1} g_{m2}} \qquad [8]$$

This is transfer function for low pass filter. Figure 8 shows passive equivalent circuit for high pass filter and transfer function for high pass is given as equation 11.Using voltage divider rule in circuit given in Figure 8, the input and output is given as:

$$\frac{V_{hp}}{V_{In2}} = \frac{Z_2}{Z_1 + Z_2} \qquad [9]$$

where $Z_2 = \dfrac{RsL}{R + sL}$ and $Z_1 = \dfrac{1}{sC_2}$ and by putting values of Z_1 and Z_2 gives following equation 10 :

$$\frac{V_{hp}}{V_{In2}} = \frac{s^2}{s^2 + s\dfrac{1}{RC_2} + \dfrac{1}{LC_2}} \qquad [10]$$

By substituting the values of L and R , the transfer function is observed as:

$$\frac{V_{hp}}{V_{In2}} = \frac{s^2 c_1 c_2}{s^2 C_1 C_2 + sC_1 g_{m2} + g_{m1} g_{m2}} \qquad [11]$$

From equation 8 and 11, the DC gain constant (*K*), the cutoff frequency, (w_o) and the quality factor (Q) of the filter are easily derived to be:

$$w_o = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}} \quad [12]$$

$$Q = \sqrt{\frac{g_{m1} C_2}{C_1 g_{m2}}} \quad [13]$$

The sensitivity of the cutoff frequency and quality factor with respect to change in passive component parameter is given by equation 14 and 15 respectively.

$$\left| S_{C_1,C_2}^{wo} \right| = \frac{1}{2} \quad [14]$$

$$\left| S_{C_1,C_2}^{wo} \right| = \frac{1}{2} \quad [15]$$

The sensitivity of filter with respect to passive components is very low. The OTA-*C* filter in Figure 5 uses a reduced number of components. The effective transconductance of OTA can be change changing the bias voltage at back gates. The biasing is provided as such to obtain high performance of circuit. The designed filter is compared with filter given in reference [J. M. Carrillo, M. A. Domínguez, J. F. Duque-Carrillo, G. Torelli(2011)].

5. Simulation results

The simulations of the proposed OTA have been performed using Tanner EDA Tool version 13.0. All the proposed design simulations are carried out at 90nm technology for high gain and wide bandwidth.

5.1 Simulation Results of Proposed OTA

The proposed circuit works at V_{DD} of 1.2 V. The control voltages are provided at back gates of M_1, M_2 and M_3, M_4 and are 0.20V and -0.58V respectively. The AC response of the proposed OTA is shown in Figure 9. The gain of 10.04 dB is observed. The gain is increased by using self cascode technique which also increases output resistance. The bandwidth is defined by the difference of lower and upper frequency at 3dB down from maximum gain and is obtained as 6 GHz. The phase responses for differential outputs of the proposed OTA are shown in Figure 10 (a) and (b). The phase margin for proposed OTA equals 96.53 degrees (180-84.47). The phase response specifies about stability of circuit. High phase margin is obtained for proposed circuit.

5.2 Simulation Results of filter

The simulations are carried out for power consumption, wide bandwidth for designed filter. The supply voltages were taken as V_{DD}= 1.2V and V_{SS}=-1.2V. The OTA circuit shown in Figure 3 is used to design filter with capacitor value of C_1=1pF and C_2=1pF. The proposed filter realizes a cut off frequency f_o of 14MHz. The ac response of filter for low pass and high pass is shown in Figure 11(a) and (b) respectively. The phase response for low pass and high pass is observed as in Figure 12(a) and (b) respectively. The phase response shows that low pass filter is lag filter because at output capacitor will take finite time to charge its plates whereas high pass filter is lead filter as capacitor is used at input node. For $g_{m1} = g_{m2} = 1sm$, high Q is obtained. Higher value of quality factor Q with very low sensitivity to parameter variation may be obtained without changing the frequency response for proposed filter. In the filter circuit all the capacitors are grounded to reduce parasitic effects and for standard integration. The circuit realizes high quality factor that is orthogonal to cut off frequency. The overall performance of all parameters of filter is given in Table I.

6. Conclusion

This paper has presented a low-power filter implemented in 90nm CMOS technology for radio frequency communication and wireless application. The main design objectives are size and low power consumption of the system. The filter circuit uses two OTAs and two capacitors. The filter shows a wide pass band of 14 MHz and power consumption of 153.4 µwatts. The proposed filter with low power and reduced number of OTA's and has large applications in VHF/UHF communication systems.

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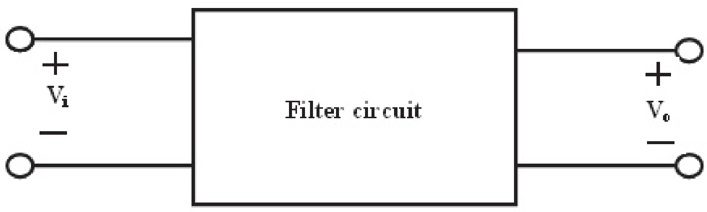


Figure1. The basic model of filter

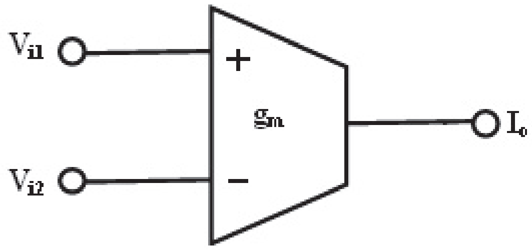


Figure 2. Block diagram of OTA

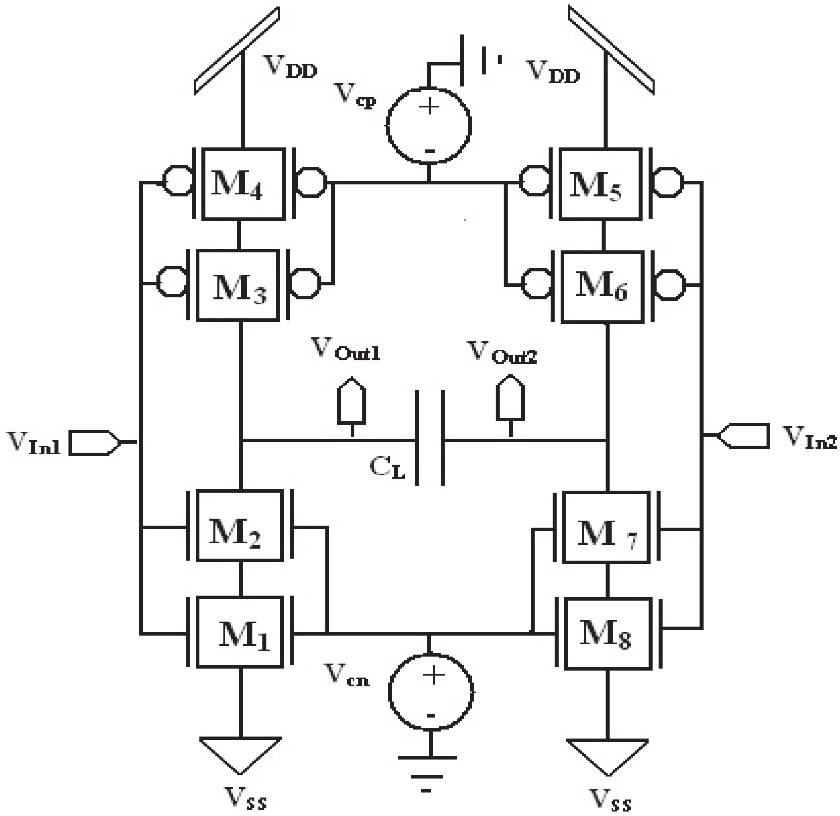


Figure 3. Proposed OTA circuit

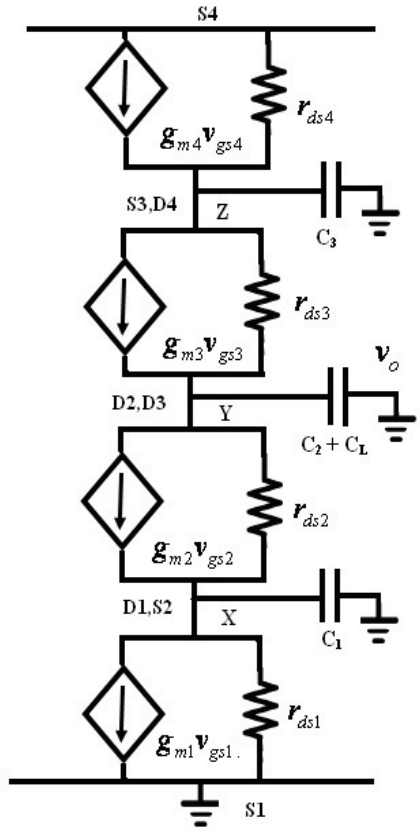


Figure 4. High frequency model of OTA

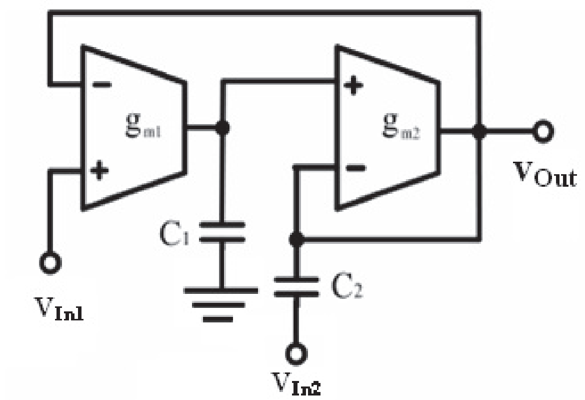


Figure 5. Circuit diagram of second order filter

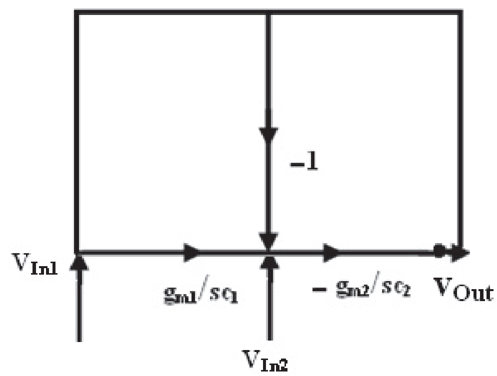


Figure 6. Signal flow graph of filter

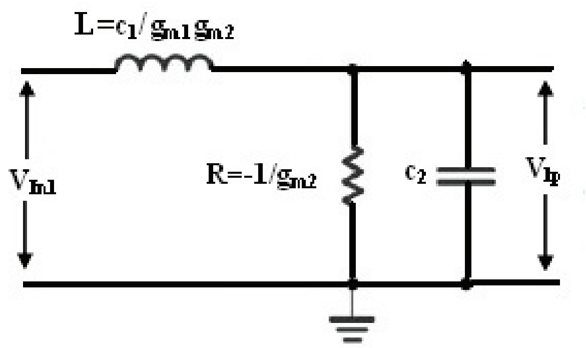


Figure 7. Equivalent circuit of passive low pass filter

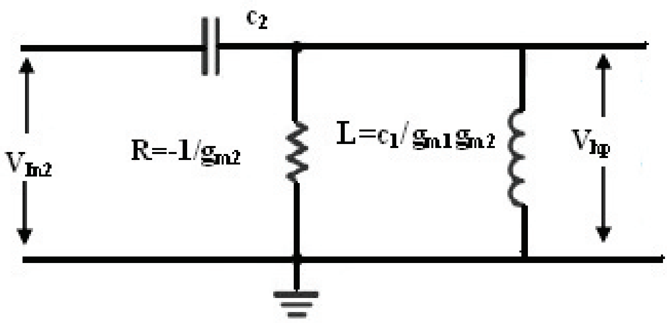


Figure 8. Equivalent circuit of passive high pass filter

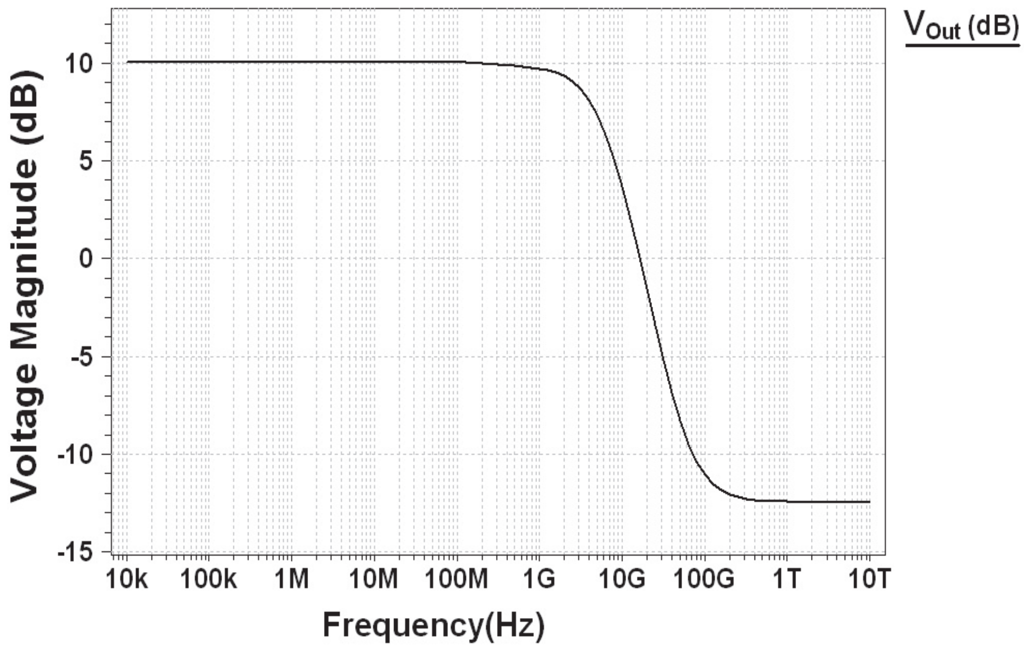
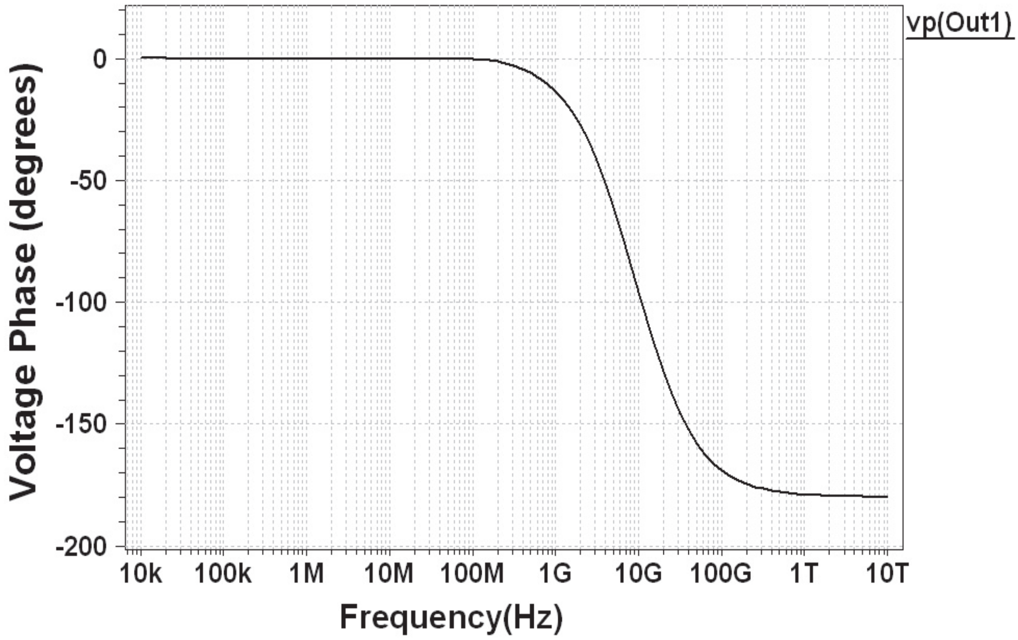
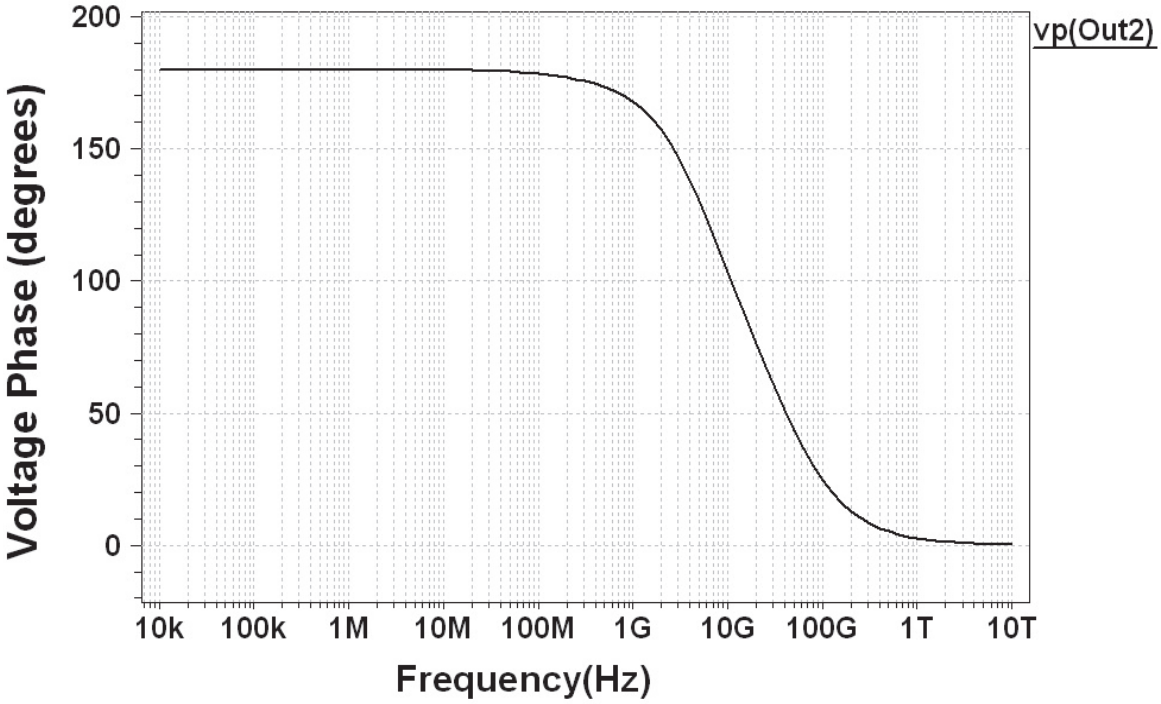


Figure 9. Differential Gain of proposed OTA

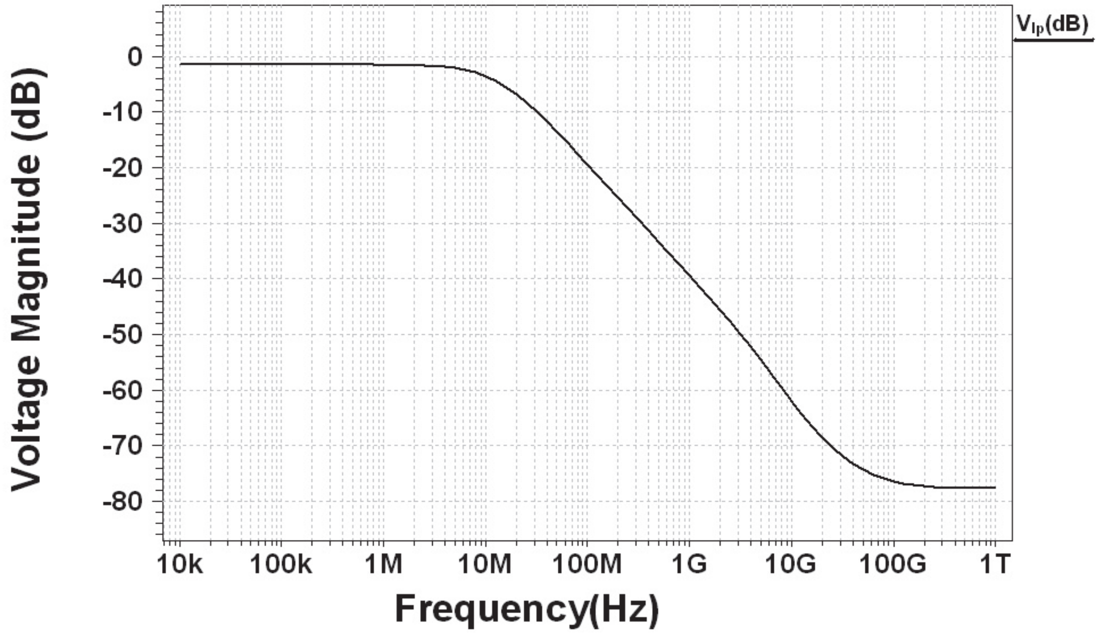


(a)

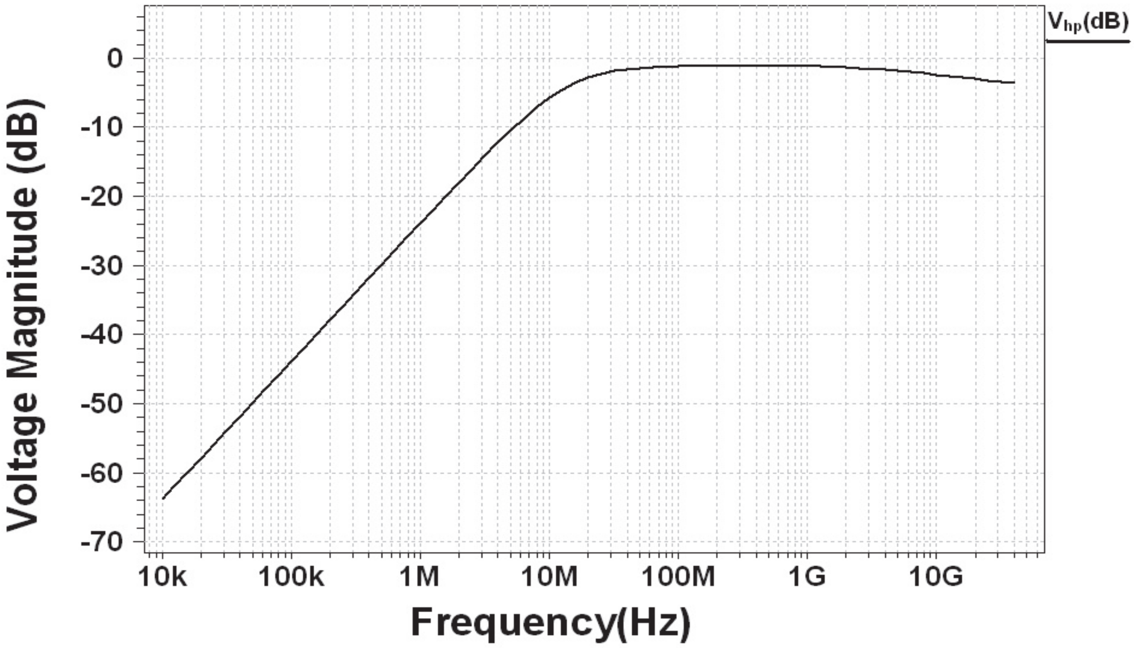


(b)

Figure 10. (a) and (b) Phase Response of proposed OTA for output V_{out1} and V_{out2} respectively

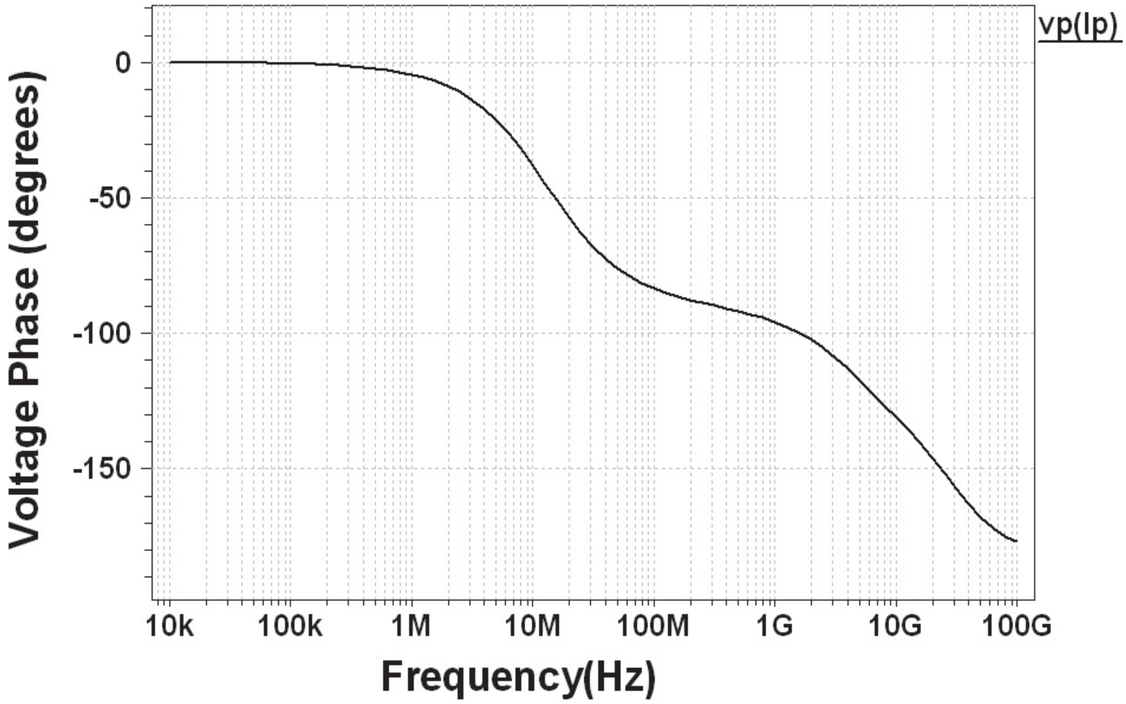


(a)

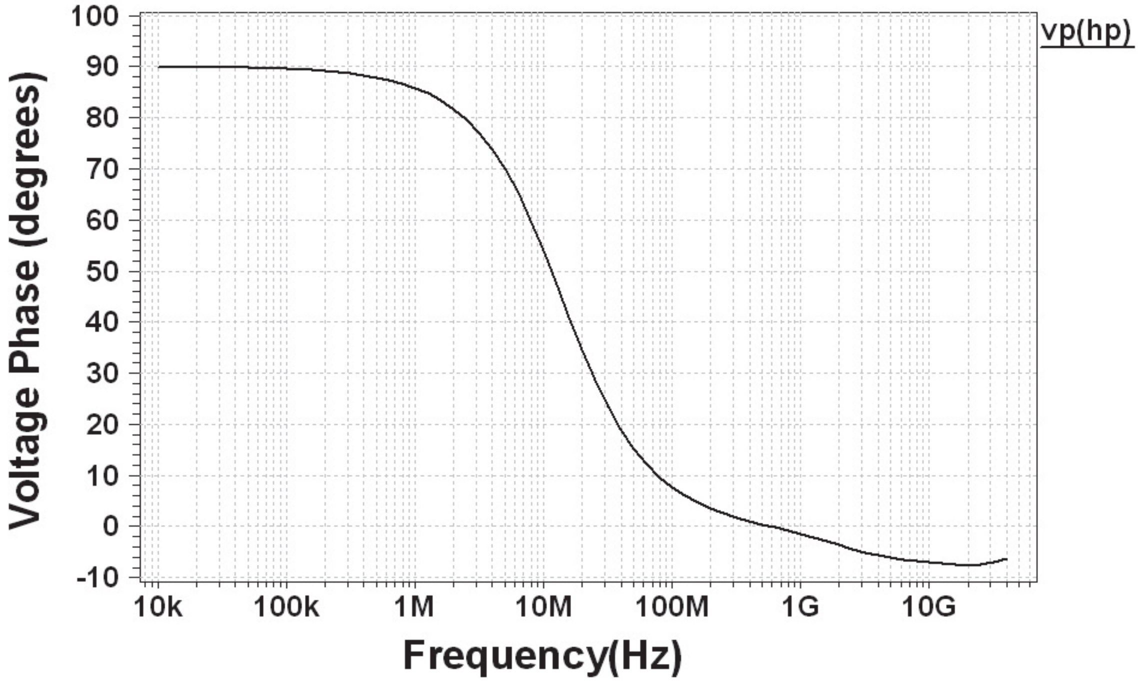


(b)

Figure 11. (a)and (b) ac response for low pass high pass at 0 dB respectively



(a)



(b)

Figure 12. (a) and (b) Phase response for low pass and high pass filter respectively

Table I. Different Parameters of Filter

Parameters	**Existing filter**	**Proposed Filter**
V_{DD}(V)	1.2	1.2
Pass band (MHz)	3	14
Q	0.5	1
Power Consumption(µwatt)	384	153.4
Number of OTA	2	2