Design of Ultra Low Power Integrated PLL using Ring VCO

Vaishali, Shruti Suman, K. G. Sharma, P. K. Ghosh

ECE Department

Faculty of Engineering and Technology

Mody University of Science and Technology

Lakshmangarh, Sikar, Rajasthan, India

shrutisuman23@gmail.com

Abstract

The design of an ultra low power Phase Locked Loop (PLL) is presented in this paper. The proposed PLL consists of a phase detector, a charge pump, low pass filter, and a ring oscillator based voltage controlled oscillator (VCO). The performance of Voltage Controlled Oscillator is of great importance for PLL. The circuit is designed using 0.13µm CMOS technology with the supply voltage of 1V and has a power consumption of 254µW.

Keywords: Charge Pump, CMOS Technology, Low Pass Filter, Phase Detector, Phase Locked Loop, Voltage Controlled Oscillator.

1. Introduction

Phase Locked loop (PLL) plays significant role in microprocessors, clock and data recovery systems, and communication devices. Due to their versatility, they have become a ubiquitous building block of modern wireless and wire-line communication systems such as wireless local area networks, mobile and satellite communication systems and back-plane interconnects etc. [Neda Nouri and Shahriar Mirabbasi (2005), Xiao Peng Yu, Manh Anh Do, Jian-Guo Ma, Wei Meng Lim, Kiat Seng Yeo, Xiao Lang Yan (2007)].

A PLL is a negative feedback system that compares reference signal with feedback signal. It is a closed loop system that fixes the relationship between output and input clock phases [Garrett Bischof, Ben Scholnick, and Emre Salman (2011)]. A phase-locked loop is basically an oscillator whose frequency is locked onto some frequency component of an input signal. It consists of a phase detector (PD) for detecting phase and a VCO in a feedback loop so that the VCO tracks the changes in the input frequency or phase and maintains the control of frequency [Harini Narayanan, Godi Fischer (2005)]. The basic block diagram of a PLL is shown in Figure 1.

The rest of the paper is organized in four different sections: Architecture of PLL is given in Section 2. Transistor level implementation of the PLL is explained in Section 3. Simulation results and transient characteristics are discussed in section 4 and finally, section 5 provides conclusion.

2. PLL Architecture

The PLL architecture basically consists of three blocks, these are: Phase detector, Low pass filter (LPF) and voltage controlled oscillator and the whole system is connected through a feedback system as shown in Figure 1. This is also called as first order PLL. This circuit does not detect frequency difference. So to eradicate this problem, phase-detector is further replaced by phase frequency detector (PFD) as shown in Figure 2. In this Figure, K_{pd} is phase detector loop gain, and $\Delta\phi$ is the phase difference between reference signal and VCO output signal [5]. In this figure, phase detector produce output that is proportional to phase difference $K_{pd}\Delta\phi$ and integral phase detector produce integral of phase difference $K_{pd}\int\Delta\phi$ dt to realize this charge pump as shown in Fig. 3. In this figure, F_{Ref}, θ_{Ref} and F_{Out}, θ_{Out} are frequency and phase of reference signal and VCO output signal, respectively.

The different parts of PLL of Figure 3 are as follows -

- Phase Detector
- Charge Pump (CP)
- Loop Filter with transfer function of Z (s)
- Voltage Controlled Oscillator with sensitivity $\frac{K_{VCO}}{s}$, where K_{VCO} is the VCO sensitivity in Hz/Volt.

3. Working Principal of PLL

In commercial PLLs, the phase detector and charge pump together form the error detector block. When $F_{Out} \neq F_{Ref}$, the error detector will fed source/sink current pulses to the low-pass loop filter. This smoothes current pulses into a voltage which, in turn, drives the VCO. The VCO frequency will then increase or decrease as our requirement by the factor of $K_{VCO}\Delta V$, where ΔV is the change in VCO input voltage. If the VCO output is lagging behind the reference signal, the phase detector will cause the charge pump to inject additional current into the low pass filter. The DC voltage at the output of the low pass filter will rise, thereby increasing the output frequency F_{Out}, of the VCO. This will continue until the error *e(s)* is zero and the loop is locked. The charge pump and VCO thus serves as an integrator, seeking to increase or decrease its output frequency to the value required so as to restore its input (from the phase detector) to zero [B .Razvi (2001)]. Once any phase or frequency differences have been eliminated, the circuit is referred to as 'locked'. In the locked condition, the output signal of a PLL can be used as a stable clock signal to recover data.

The schematic diagram of proposed PLL is shown in Figure 4. The PLL compares the input data stream (reference signal) with the output of the voltage controlled oscillator (VCO) using a phase detector (PD). Any difference in the phase of the two inputs of the PD causes a predictable output signals that are 'UP' and 'DOWN' signal, which are used by the charge pump (CP) to either charge or discharge the capacitors in the low pass filter (LPF). Then VCO controls output frequency according to the applied control voltage.

4. Circuit Implementation

The transistor level implementation of the PFD, CP, and VCO are designed using 0.13μm CMOS with a reduced power supply of 1V.

4.1 Phase Detector

The Phase Detector generates UP/DOWN pulses according to the phase difference between the positive edges of reference signal and output signal of VCO [Y. C. Chen, F. R. Chang and Y. S. Chou (2010)]. The Phase detector is constructed using two D-flip-flops (D-FF) and conventional NOR gate as shown in Figure 5 [Garrett Bischof, Ben Scholnick, and Emre Salman (2011), Sinisa Milicevic and Leonard MacEachern (2008)]. These D-FFs are RESET when there is logic high at the RESET input, and the output signal after RESET is also logic high.

The design of phase detector is shown in Figure 6. When RESET becomes 'one', M2 and M6 are enabled then M3 and M7 are ON and UP signal returns to logic high. Similarly DOWN pulse returns to 'one'. If reference signal goes 'zero' to 'one', M4 is enabled and UP pulse returns to 'one' and when VCO signal is one, and M8 gets enabled and DOWN pulse returns to 'one'. When reference signal leads VCO signal, phase difference is indicated by UP pulse and if VCO signal is leading the reference signal, then phase difference is indicated by DOWN pulse.

4.2 Charge Pump with Low Pass Filter

The charge pump is incorporated into the PLL design in order to increase the acquisition range of the circuit [Garrett Bischof, Ben Scholnick, and Emre Salman (2011), Zuoding Wang (2005)]. The schematic diagram of charge pump with low pass filter is shown in Figure 7. In this circuit M1 and M4 act as current source. When there is a 'zero' in the UP pulse, the pMOS transistor in the charge pump closes and the top current source charges capacitor C. When the DOWN pulse is a 'zero', the zero gets inverted and produces 'one' at the input of the nMOS transistor. This signal closes the nMOS transistor and the lower current source discharges the capacitor. The final design has power consumption 1.401μW.

4.3 Voltage Controlled Ring Oscillator

The VCO is most commonly used in clock recovery circuits in digital communication and on-chip clock distribution etc [Hesieh Y. B. and Kao Y. H. (2008), Anand S. S.B. and Razavi B. (2001)]. In its most standard form the output frequency of VCO is a linear function of its input control voltage as given by equation (1):

$$f_{Out} = f_o + K_{VCO}V_{ctrl} \qquad (1)$$

where, f_o is the free-running frequency of the VCO, V_{ctrl} is the input control voltage and K_{VCO} is the sensitivity or gain of the VCO which controls output frequency of VCO. V_{ctrl} is the input to the VCO that sets it to the desired frequency [Stephen Docking (2002)].

The VCOs can be designed as LC circuits and as ring oscillators (ROs). Ring oscillators are often used in high-speed digital circuits for clock generation. Several reasons justify this popularity; one of them is wide tuning

range, which can be easily obtained with a ring oscillator and another reason is, its compatibility with digital CMOS technology. Along with these advantages, it occupies substantially less area than LC oscillators [Shruti Suman, Monika Bhardawaj & Prof. B.P.Singh (2012)].

In modern communication systems, power consumption and frequency tuning are key performance metric. Growing demand of portable devices like cellular phones, personal communication devices have drawn attention for the low power consumption. Total power consumption P_{total} in MOS logic circuits is given as equation (2):

$$P_{total} = P_s + P_d + P_{sc} \qquad (2)$$

where, P_s, P_d and P_{sc} are the static, dynamic and short circuit power dissipation respectively [Kang, S and Leblebici , Y. (2003)].

Dynamic power dissipation results from switching of load capacitance between two logics and depends on frequency of operation, whereas static power is contributed by the direct short circuit current path between supply voltage and ground which depends on leakage current. Controlling the bulk terminal of CMOS device offers improved performance in term of power dissipation In VLSI design, power and delay are the figure of merit during the selection and implementation of a device in chip fabrication. To reduce the standby leakage in CMOS circuits, a reverse body biasing is generally used.

The schematic view of proposed ring VCO is shown in Figure 8. In this circuit, output frequencies of VCO have been controlled by varying the reverse bias voltage which also provides significant improvement in power consumption. The power consumption is reduced because of reverse substrate bias voltage. The body biasing is used to control threshold voltage V_t. The effect of substrate bias voltage V_{SB} on the channel can be most conveniently represented as a change in the threshold voltage V_t as given by equation (3):

$$V_t = V_{to} + \gamma \left(\sqrt{|V_{SB} - 2\phi_F|} - \sqrt{|2\phi_F|} \right) \qquad (3)$$

here, V_{to} is the zero-bias threshold voltage, γ refers to the body-effect coefficient, V_{SB} is substrate bias voltage and φ_F represents the quasi-fermi potential. By changing the substrate bias voltage, the threshold voltage of the circuit can be changed. Threshold voltage affects the drain current. The variation in drain current, changes drain to source resistance of pMOS and nMOS transistors. So charging and discharging times can be varied according to body bias voltage and output frequency has been controlled by control voltage that is same as the reverse bias voltage applied at bulk terminal. If control voltage increases the threshold voltage also increases and hence the drain current decreases resulting in the source to drain resistance to increase. This results in a decrease in the output frequency [Vaishali, Shruti Suman, K. G. Sharma, P. K. Ghosh (2014)].

5. Simulation Results
The simulations of the proposed and the existing designs have been performed using Tanner EDA Tool version 13.0. The proposed designs simulations are performed on 130nm CMOS technology with supply voltage 1V.

5.1 The Input Output waveforms of Phase Detector
The Phase Detector is one of the most important parts of PLL that detects the phase difference between reference signal and VCO output signal [Yifei Luo, Kuan Zhou (2007)]. The phase detector circuit can be analyzed in three different ways:

- Reference signal leads VCO signal
- Reference signal lags VCO signal
- Reference signal is in phase with VCO signal.

In the first case, the UP pulse represents the difference between the phases of two clock signals. As shown in Figure 10, V_{Ref} is leading V_{VCO}, this means that the VCO needs to speed up to match V_{Ref}. Figure 10 also shows more zeros in the UP signal than the DOWN signal, this corresponds to an increase in the VCO control voltage as well as the VCO output frequency.

In the second case as shown in Figure 11, reference signal is lagging with VCO signal. In this DOWN pulse represents the difference between the phases of two clock signals.

In the third case as shown in Figure 12, ref signal is in phase with VCO signal. When the PLL is locked, UP and DOWN signals become a nearly constant logic high value. The final design has a power consumption of approximately 0.236mW.

5.2 Input-Output waveforms of Charge Pump

The charge pump (CP) is used to charge or discharge the capacitors of the low pass filter (LPF) according the outputs (UP and DOWN) of Phase Detector. When UP pulse is logic low, the CP charges the capacitor C, thereby rise up the output voltage, as shown in Figure 13.

5.3 Simulation Results of Proposed Voltage Controlled Ring Oscillator

In the proposed three stage ring VCO of Figure 8, reverse bias voltage is applied at bulk terminal of nMOS and pMOS transistors. Hence the output frequencies of VCO have been controlled by varying the reverse bias voltage which also reduces power consumption. The output waveform of proposed three stages ring VCO of Figure 8 is shown in Figure 14. Table I shows results for proposed three stages Ring VCO. Control voltage has been varied from 3.2V to 0.4V and we observe the output frequency which ranges from 917.43MHz to 4189.53 MHz with deviation in power consumption from 3.61μW to 29.21μW. We have selected this range of control voltage because output frequency shows linear behaviour in this range. The control voltage is varied in negative direction because of reverse body bias voltage is applied. The output waveform of the circuit of Figure 8 is shown in Figure 14(a) while the output waveform for layout diagram of Figure 9 is shown in Figure 14(b).

Figure 15 and 16 show output frequency and power consumption variation with control voltage. Almost liner relation between control voltage and frequency of oscillation is observed. As control voltage increase, output frequency and power consumption also increases.

5.4 Simulation Results of PLL

The proposed PLL has been simulated at the transistor-level and some results are discussed in this section. The power consumption is given in Table II. The total power consumption of PLL is 236μW. As shown in Figure 17 and Figure 18, the output frequency and phase are locked by input clock pulses. Figure 17 is for low frequency clock and Figure 18 corresponds to high frequency clock. The Proposed PLL shows better performance in terms of power consumption, VCO tuning range as shown in Table IV.

6. Conclusion

This paper has presented a low-power PLL implemented in 0.13μm CMOS technology for communication systems. The PLL is used to generate a stable clock signal at each mode of the receiver. The Improved power efficient design of PLL consists of a phase detector; a charge pump, low pass filter, and bulk driven ring VCO. The proposed ring VCO shows better performance in terms of tuning range (917.43 MHz-4189.53 MHz) and power consumption. The key design objectives of PLL are size, power consumption, lock range, frequency range and the signal acquisition ability of the system. The proposed low power, small area PLL has great potential in implantable biomedical and wireless systems.

Reference

Neda Nouri and Shahriar Mirabbasi (2005), "A 900MHZ-2GHZ Low-Swing Low-Power 0.18μM CMOS PLL"*IEEE Digital Library*, 1566 – 1569.

Xiao Peng Yu, Manh Anh Do, Jian-Guo Ma, Wei Meng Lim, Kiat Seng Yeo, Xiao Lang Yan (2007), " Sub-1V Low power Wide Range Injection Looked Frequency divider" Microwave and Wireless components letters, *IEEE*, Vol.-17, 528-530.

Garrett Bischof, Ben Scholnick, and Emre Salman (2011)," Fully Integrated PLL Based Clock Generator for Implantable Biomedical Applications "in *System Application & Technology Conference, IEEE digital Library*, 1 - 4.

Harini Narayanan, Godi Fischer (2005), "Ultra Low Power Phase Looked Loops" Circuit and Systems , *IEEE digital Library ,*1370- 1373.

B .Razvi (2001), Design of Analog CMOS Integrated Circuits , *McGraw- Hill*.

Y. C. Chen, F. R. Chang and Y. S. Chou (2010), " Loop Filter design of third order charge pump PLL using Linearized discrete Time model", *IEEE International Conference on Control Application*, 2225-2230.

Sinisa Milicevic and Leonard MacEachern (2008), "A Phase Frequency Detector and A Charge Pump Design for PLL Applications" *IEEE International Symposium on Circuit and Systems*, 1532-1535.

Zuoding Wang (2005), "An analysis of charge-pump phase-locked loops" *IEEE digital library,* 2128 – 2138.

Hesieh Y. B. and Kao Y. H. (2008), " A Fully integrated spread-spectrum clock generator by using direct VCO modulation," *IEEE Trans. Circuit Systems*, Vol. 55, 1845-1853.

Anand S. S.B. and Razavi B. (2001), "A CMOS clock recovery circuit for 2.5-Gb/s NRZ data, "*IEEE J. Solid-State Circuit*, Vol. 36, 432–439.

Stephen Docking (2002), " A Method to Derive an Equation for the Oscillation Frequency of a Ring Oscillator", A Thesis of Master of Applied Science.

Shruti Suman, Monika Bhardawaj & Prof. B.P.Singh (2012) , "An Improved Performance Ring Oscillator Design" in *International Conference on Advance Computing and Communication Technology*, Rohtak, India, *IEEE digital library,*236-239.

Kang, S and Leblebici , Y. (2003), "CMOS Digital Integrated Circuits", *TMGH*.

Vaishali, Shruti Suman, K. G. Sharma, P. K. Ghosh (2014), " Design of Ring Oscillator based VCO with improved performance ", *Innovative Systems Design and Engineering* ,Vol. 5.No-2, 31-41.

Yifei Luo, Kuan Zhou (2007), " A 24 GHz Multi Phase PLL for Optical Communication", Circuit and Systems, *IEEE digital library*, 461-464.

Ms. Vaishali is persuing M.Tech. from Mody University of Science and Technology, Lakshmangarh, Sikar, Rajasthan, India. She has completed her B. Tech. from College of Engineering and Technology, Bikaner, India, in the year 2012. Her Research Interests are in VLSI Design. She has over 2 papers to her credits in International Journals /Conferences.

Ms. Shruti Suman did M.Tech. from Mody Institute of Technology and Science Lakshmangarh, Sikar, Rajasthan, India in the year 2012. She has completed B.E. from Rajeev Gandhi Technical University, Bhopal, India, in the year 2010. Her Research Interests are in Analog and Digital VLSI Design. From 2012 till date, she is Assistant Professor in ECE Department, Mody University of Science and Technology, Lakshmangarh, Sikar, Rajasthan (India). She has over 10 papers to her credits in International Journals /Conferences including IEEE.

Dr. K. G. Sharma received the B.E. degree in Electronics and Communication Engineering from Madan Mohan Malviya Engineering College, DDU University, Gorakhpur in 2001 and completed M .Tech. in VLSI design from, Mody Institute of Technology and Science ,Lakshmangarh, Sikar, Rajasthan, India in the year 2009. He has completed Ph.D. degree in the field of low power VLSI circuits from from Suresh Gyan Vihar University, Jaipur. He demonstrated his skills in Research & Development of Industrial Electronics, Kanpur for a briefer period and then he shifted to Academics. He extended his profession as Assistant Professor in Mody University of Science and Technology, Lakshmangarh, Sikar, Rajasthan (India). He has more than 40 research papers published in various international/ national journals and conferences. He is the life member of Indian Society of Technical Education (ISTE).

Dr. P. K. Ghosh was born in Kolkata, India in 1964. He received his B.Sc (Hons in Physics), B.Tech and M.Tech degrees in 1986, 1989, and 1991, respectively from Calcutta University. He earned Ph.D.(Tech) degree in Radio Physics and Electronics in 1997 from the same University. He served various institutions, namely, National Institute of Science and Technology (Orissa), St. Xavier's College (Kolkata), Murshidabad College of Engineering and Technology (West Bengal), R. D. Engineering College (Uttar Pradesh) and Kalyani Government Engineering College (West Bengal) before he joins Mody University of Science and Technology (Rajasthan). To his credit, he has more than 30 research papers in Journals of repute and conference proceedings. He is life member of Indian Society for Technical Education (ISTE), New Delhi. His research interests are in the areas of reduced order modelling, VLSI circuits & devices, wireless communications and signal processing.
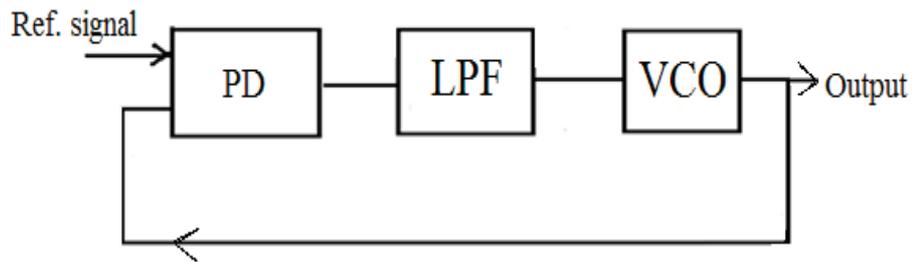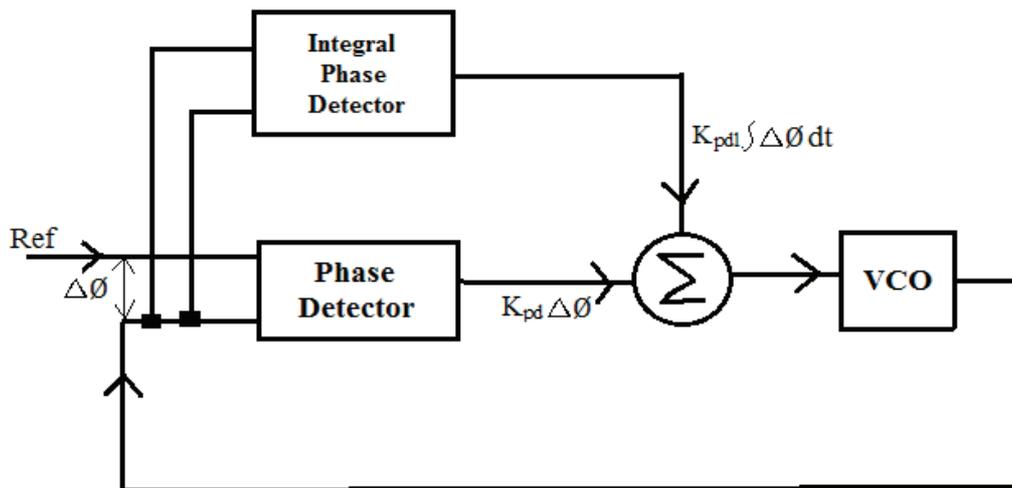
Figure 1. The Basic model of PLL

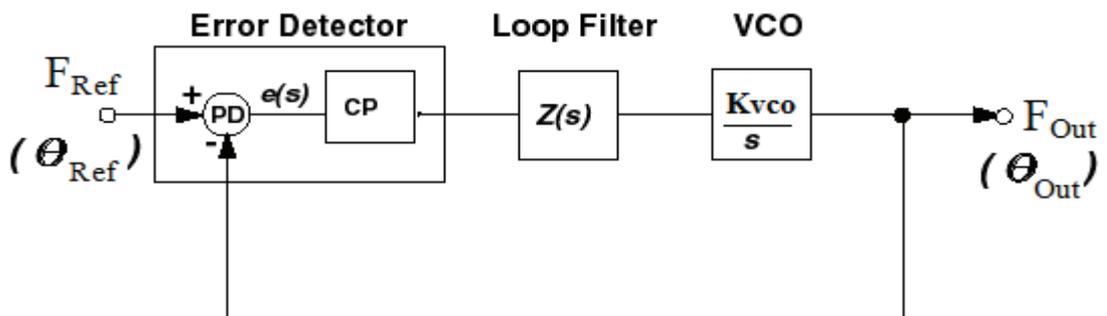Figure 2. Addition of frequency detection in phase looked loop

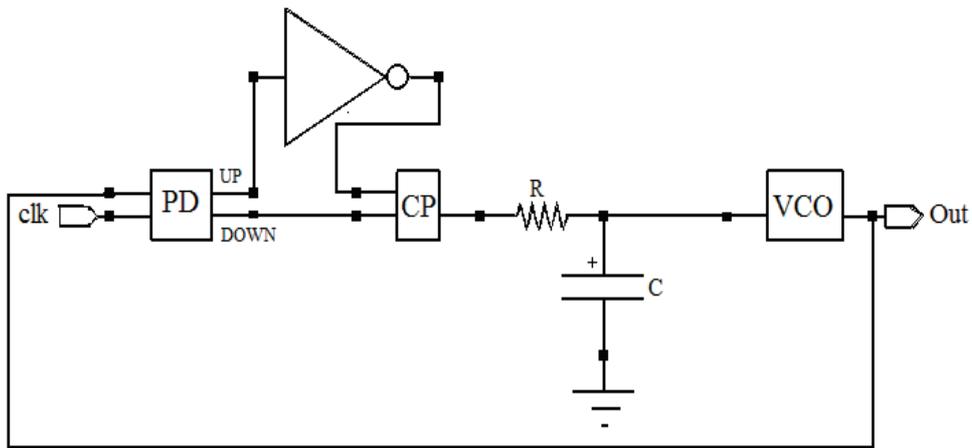Figure 3. The block diagram of phase looked loop model
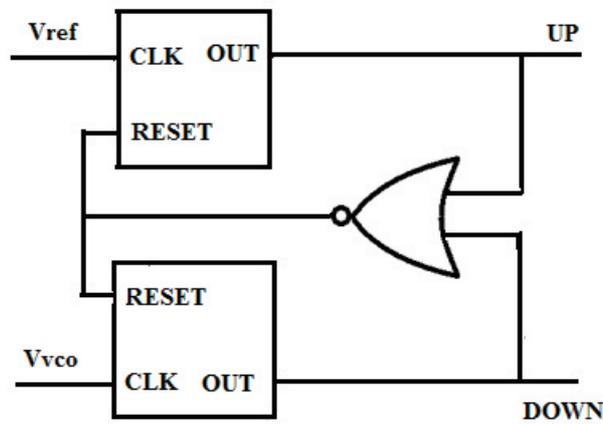
Figure 4. Linear model of ring oscillator

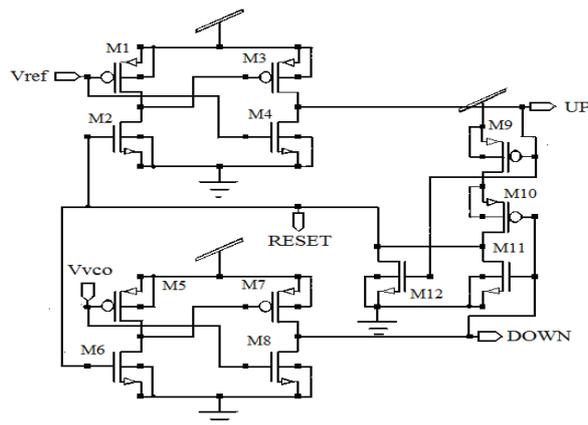Figure 5. Block diagram of phase detector

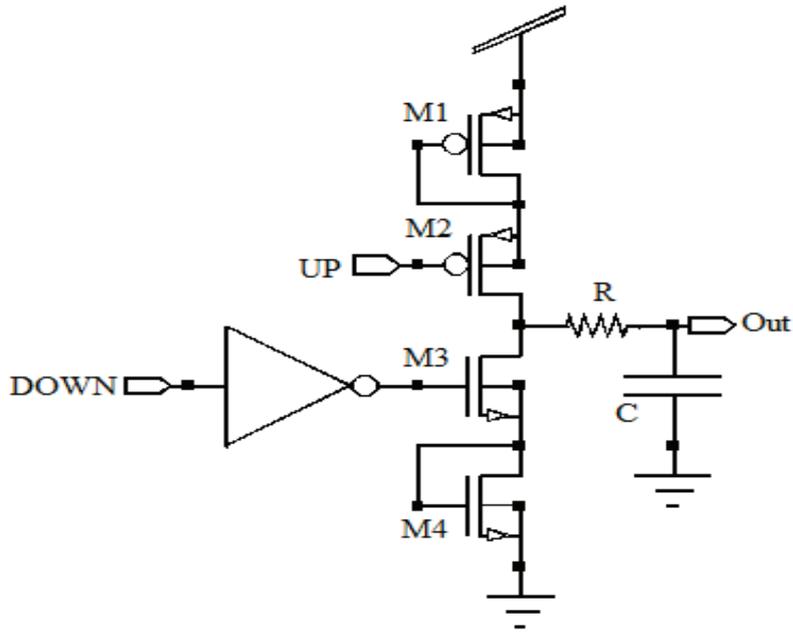

Figure 6. Schematic diagram of Phase Detector

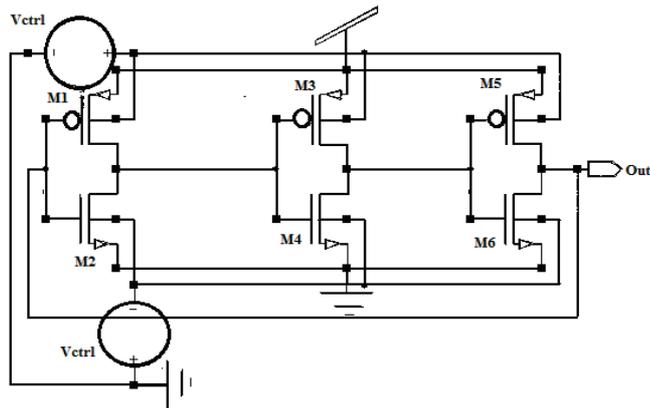Figure 7. Schematic diagram of charge pump with low pass filter

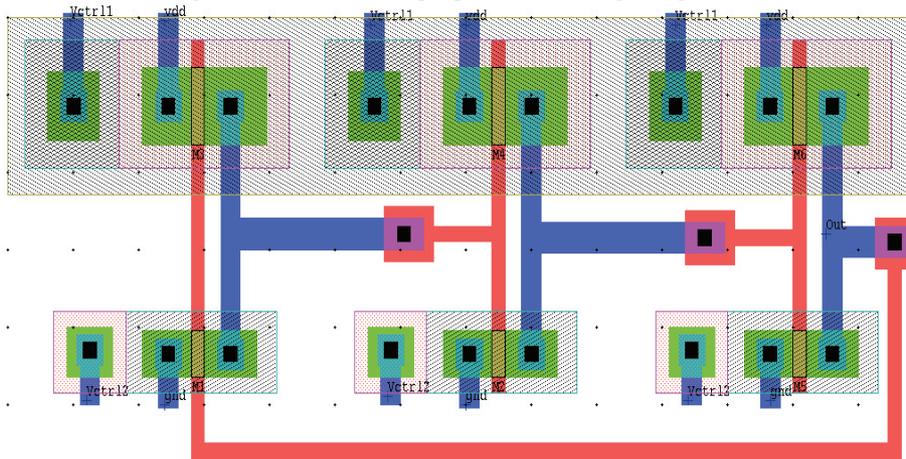Figure 8. Schematic of proposed three stage ring VCO
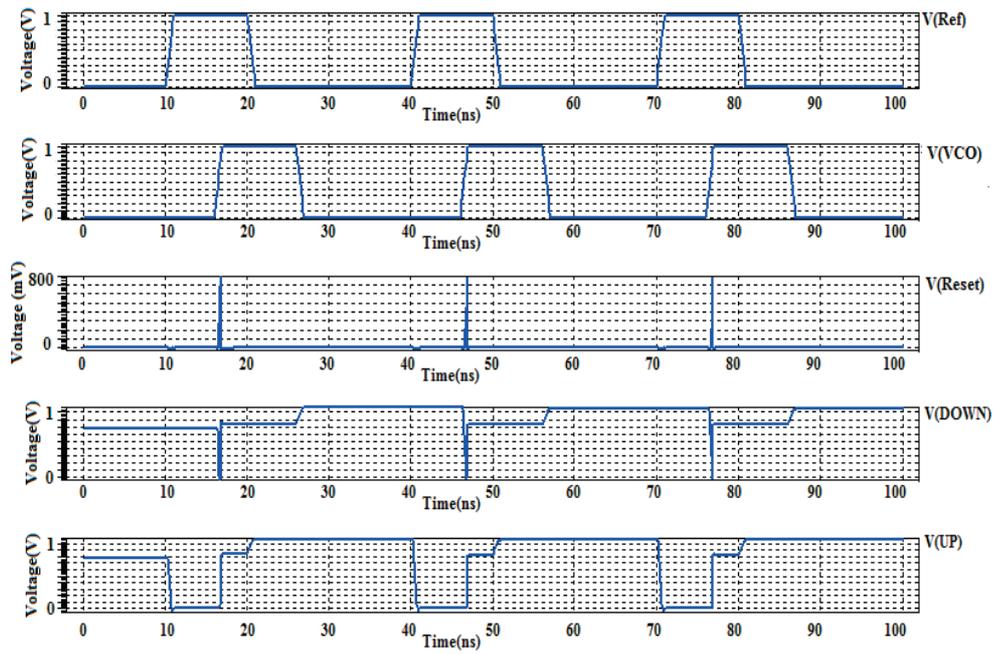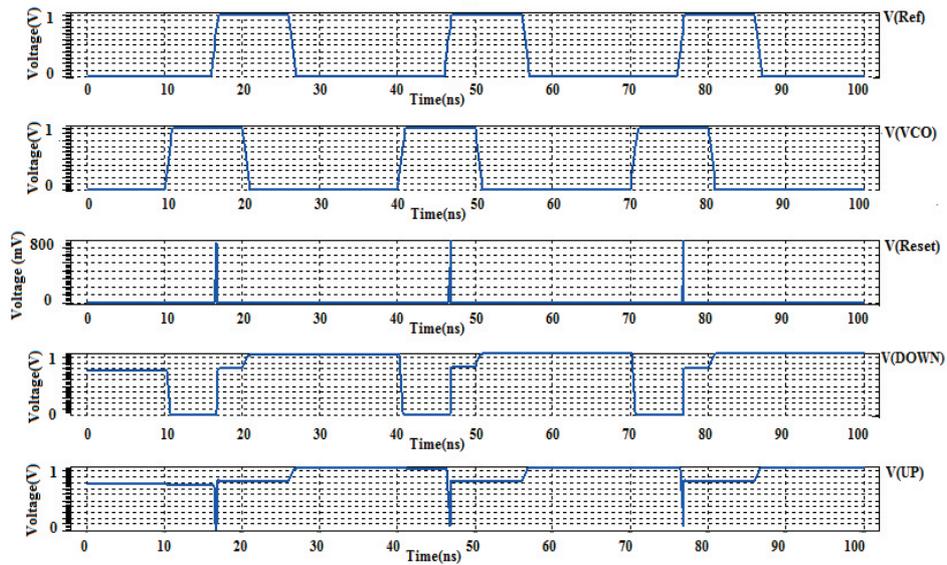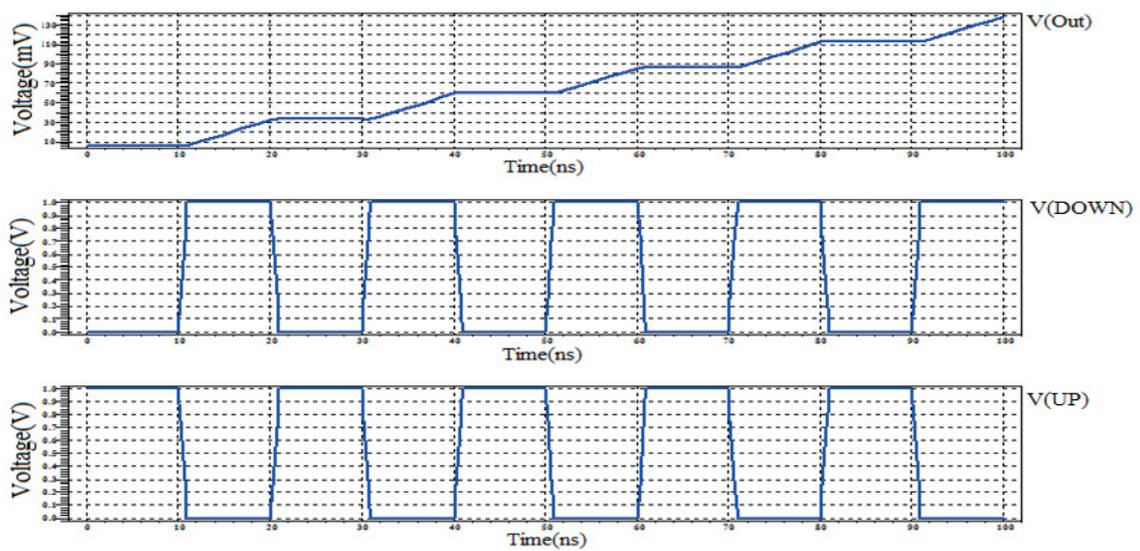

Figure 9. Layout of proposed VCO

Figure 10. Input-output waveforms of phase detector when reference signal is leading with VCO signal
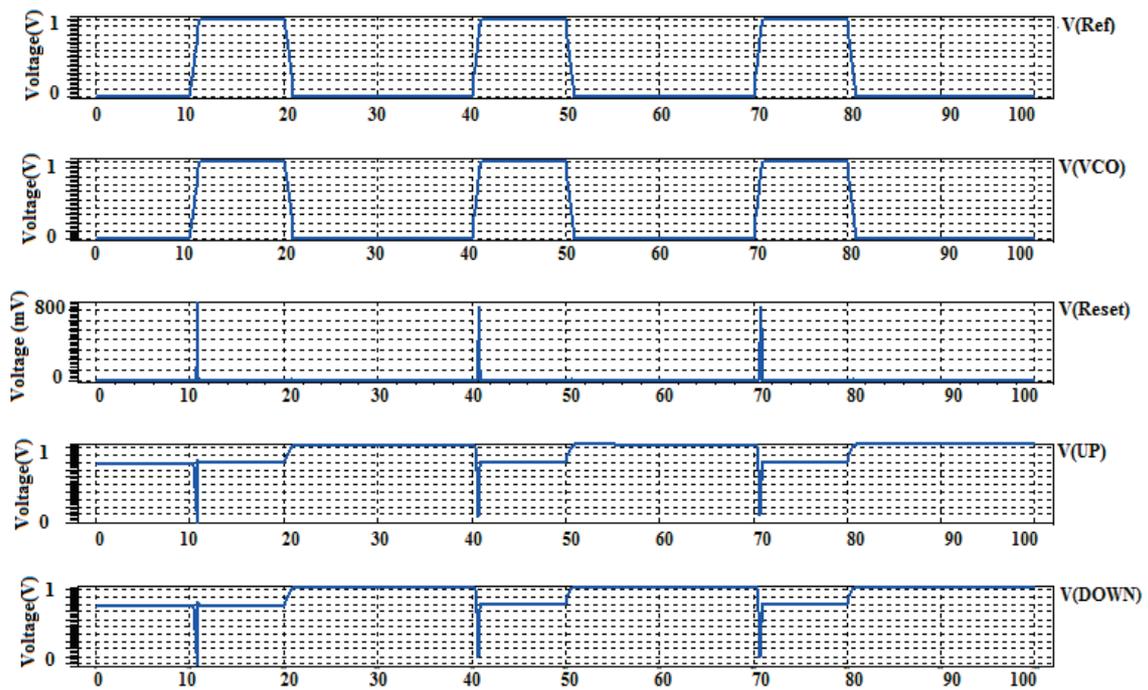
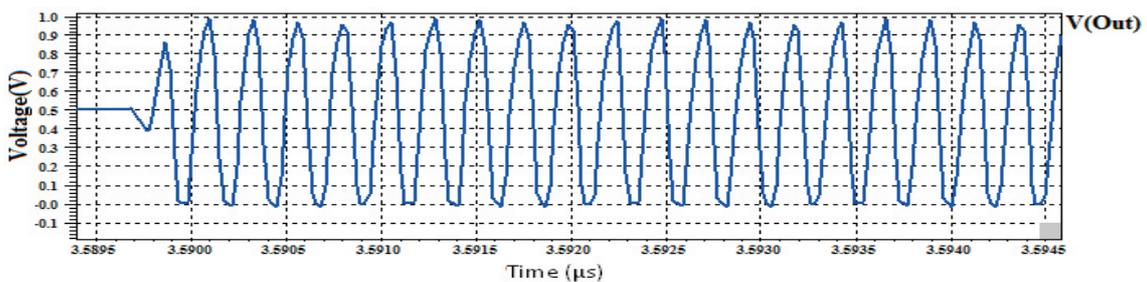Figure 11. Input- output waveforms of phase detector when reference signal is lagging with VCO signal

Figure 12. Input - output waveforms of phase detector when reference signal is in phase with VCO signal

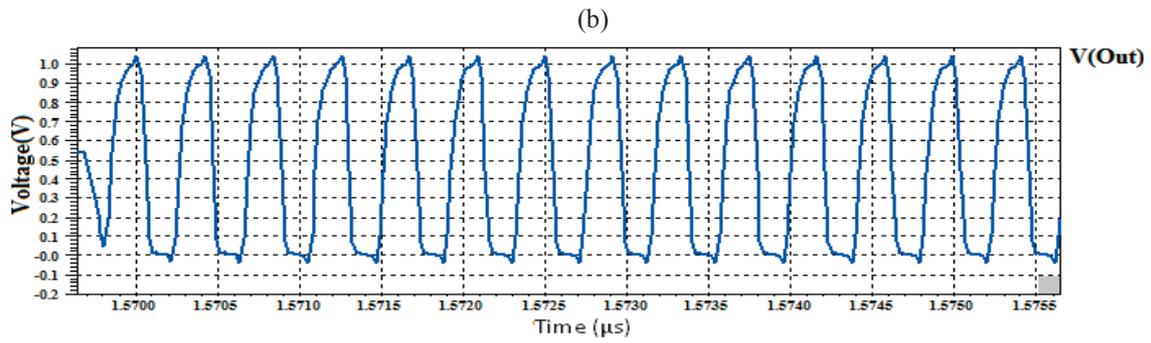Figure 13. The Input – output waveform of charge pump

(a)

(b)

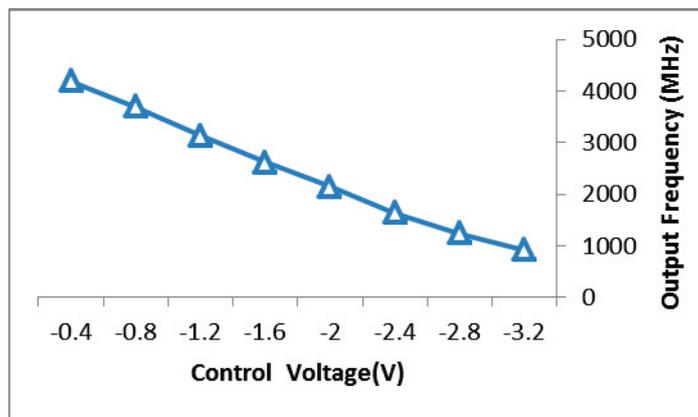Figure 14 (a) and (b). Output waveform of schematic and layout of proposed three stage Ring VCO

Figure 15. Variations of Output frequency with control voltage
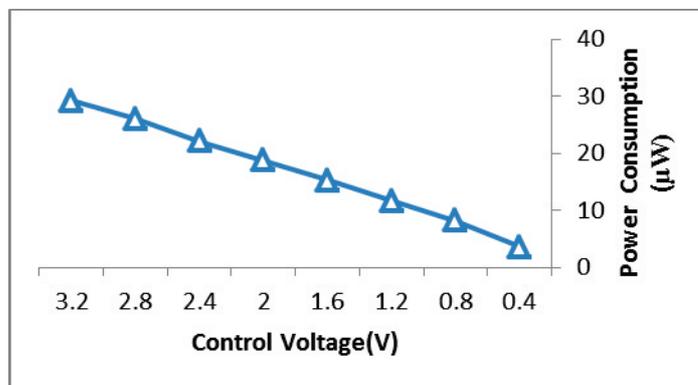

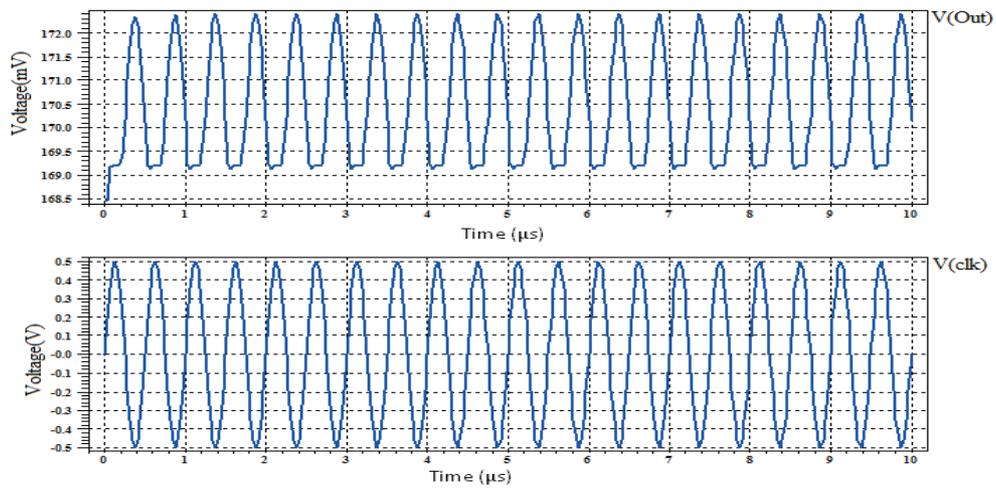Figure 16. Variations of Power consumption with control voltage

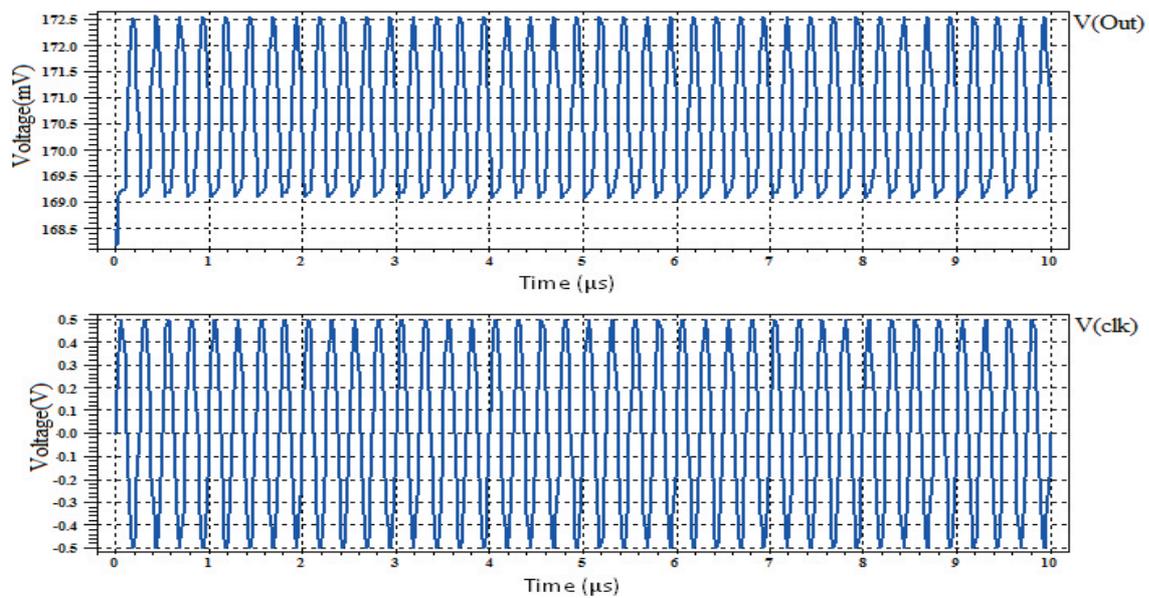Figure 17. Input-Output waveform of PLL at low frequency

Figure 18. Input-Output waveform of PLL at high frequency

Table I. Simulation results for proposed three stage Ring VCO

Control Voltage (V)	Output Frequency (MHz)	Power Consumption (μW)
3.2	917.43	3.61
2.8	1245.90	8.20
2.4	1634.28	11.68
2.0	2147.02	15.26
1.6	2615.06	18.70
1.2	3138.04	22.16
0.8	3691.80	26.05
0.4	4189.53	29.21

Table II. Power consumption of each PLL block

Block	Power Consumption(μW)
Phase Detector	236
Charge pump and Low pass filter	1.401
VCO	16.85

Table III. Parameters value of Proposed PLL

Parameters	Value
Total Power Consumption	254μW
Lock period	10ns-10μs
Noise level	1.8628mV
No of Transistor	22
VCO Frequency Range	917.43 MHz-4189.53 MHz

Table IV. Comparative Analysis of Existing and Proposed PLL

Parameters	Existing PLL (Reference no. 3)	Proposed PLL
Total Power Consumption	492 μW	254 μW
No of Transistor	30	22
VCO Tuning Range	1KHz -15MHz	917.43 MHz-4189.53 MHz

The IISTE is a pioneer in the Open-Access hosting service and academic event management. The aim of the firm is Accelerating Global Knowledge Sharing.

More information about the firm can be found on the homepage:
http://www.iiste.org

CALL FOR JOURNAL PAPERS

There are more than 30 peer-reviewed academic journals hosted under the hosting platform.

Prospective authors of journals can find the submission instruction on the following page: http://www.iiste.org/journals/ All the journals articles are available online to the readers all over the world without financial, legal, or technical barriers other than those inseparable from gaining access to the internet itself. Paper version of the journals is also available upon request of readers and authors.

MORE RESOURCES

Book publication information: http://www.iiste.org/book/

Recent conferences: http://www.iiste.org/conference/

IISTE Knowledge Sharing Partners

EBSCO, Index Copernicus, Ulrich's Periodicals Directory, JournalTOCS, PKP Open Archives Harvester, Bielefeld Academic Search Engine, Elektronische Zeitschriftenbibliothek EZB, Open J-Gate, OCLC WorldCat, Universe Digtial Library , NewJour, Google Scholar