Wallace Tree Multiplier Designs: A Performance Comparison Review

Himanshu Bansal, K. G. Sharma*, Tripti Sharma

ECE department, MUST University, Lakshmangarh, Sikar, Rajasthan, India

*sharma.kg@gmail.com

Abstract

Multiplication process is often used in digital signal processing systems, microprocessors designs, communication systems, and other application specific integrated circuits. Multipliers are complex units and play an important role in deciding the overall area, speed and power consumption of digital designs. This paper presents a comparison review of various Wallace tree multiplier designs in terms of parameters like latency, complexity and power consumption.

Keywords: Booth Recoding Algorithm, Carry Look Ahead Adder, Carry Select Adder, Compressors, Ripple Carry Adder, Sklansky Adder, Wallace Tree Multipliers**.**

1. Introduction

Multipliers have gained the significant importance with the introduction of the digital computers. Multipliers are most often used in digital signal processing applications and microprocessors designs. In contrast to process of addition and subtraction, multipliers consume more time and more hardware resources. With the recent advances in technology, a number of multiplication techniques have been implemented for fulfilling the requirement of producing high speed, low power consumption, less area or a combination of them in one multiplier. Speed and area are the two major constraints which conflict each other. Therefore, it is the designer's task to decide proper balance in selecting an appropriate multiplication technique as per requirements.

Parallel multipliers are the high speed multipliers. Therefore, the enhanced speed of the multiplication operation is achieved using various schemes and Wallace tree is one of them [1]. There are three phases in the multiplier architecture:

1. The first phase is the generation of partial products;

2. Accumulation of partial product in second phase; and

3. The third phase is the final addition phase.

In this paper, several types of Wallace tree multipliers are studied which have reduced complexity, power consumption and latency as compared to the conventional Wallace tree multiplier[2][3][5][6]. This paper is organized as follows. Section II presents the conventional Wallace tree multiplier. A reduced complexity Wallace multiplier reduction approach, a novel low power and high speed Wallace tree multiplier, Booth recoded Wallace tree multiplier, and an efficient high speed Wallace tree multiplier are described and compared with the conventional Wallace tree multiplier in section III, IV, V, and VI respectively. Section VII summarizes the conclusion.

2. Conventional Wallace Reduction Method

Wallace multiplier [1] is an efficient parallel multiplier. In the conventional Wallace tree multiplier, the first step is to form partial product array (of N^2 bits). In the second step, groups of three adjacent rows each, is collected. Each group of three rows is reduced by using full adders and half adders. Full adders are used in each column where there are three bits whereas half adders are used in each column where there are two bits. Any single bit in a column is passed to the next stage in the same column without processing. This reduction procedure is repeated in each successive stage until only two rows remain. In the final step, the remaining two rows are added using a carry propagating adder. An example of a representation of the conventional 8-bit by 8-bit Wallace tree multiplier is shown in Figure 1. The three row groupings are shown by light lines.

In a conventional Wallace multiplier, the number of rows in subsequent stages can be calculated as:

$$r_{i+1} = 2[r_i/3] + r_i \bmod 3 \tag{1}$$

Where, $r_i \bmod 3$ denotes the smallest non-negative remainder of $r_i/3$. The number of rows in the subsequent

stages of a conventional 8-bit by 8-bit Wallace multiplier are calculated using (1), that are: r_0=N=9, r_1=6, r_2=4, r_3=3, r_4=2. Therefore, four stages are required to perform the reduction procedure, each with delay of one full adder.

3. A Reduced Complexity Wallace Multiplier Reduction Approach

Waters et al. presented reduced complexity Wallace multiplier reduction approach [2]. It is a modification to the second phase reduction method used in the conventional Wallace multipliers, in which number of the half adders is greatly reduced. In the first phase, the partial product array is formed and it is converted in the form of an inverted pyramid array. An inverted pyramid array is formed when the bits in the left half of the partial product array is shifted in the upward direction. In the second phase, this array is divided into group of three rows each and full adders are used in each column. Half adders are used only when the number of reduction stages of the modified Wallace multiplier is exceeding that of the conventional Wallace multiplier.

According to equation (1) in the modified Wallace multiplier, if (r_i mod 3) = 0, then half adder is needed in the reduction stage otherwise half adder is not required. The number of half adders was observed to be (N-S-1). In the modified Wallace 9 by 9 bit reduction, only one half adder is used in the first and the second phase and two half adders are used in the final phase as shown in Figure 2. In the third phase, (2N-2) bit carry propagating adder is used. Therefore, we observed that the number of the reduction stages remain same as compared to the conventional Wallace reduction whereas two more full adders and 17 fewer half adders are used in the modified Wallace multiplier.

Both the modified and the conventional Wallace multipliers are compared for sizes from 8 to 64 bits as shown in Table 1. Both multipliers yield same performance in the terms of delay and have same number of the reduction stages, but the modified Wallace multiplier has the advantage of reduced complexity as number of half adders is 80% less than the conventional Wallace multiplier in the second phase. However due to reduction in number of half adders, the total gate count in modified Wallace reduction is always less than that of the conventional Wallace reduction. The number of full adders is somewhat increased between 1-5 for 8-64 bit modified Wallace multiplier.

4. A Novel Low Power and High Speed Wallace Tree Multiplier for RISC Processor

Vinoth et al. proposed new design of Wallace multiplier. Multi bit compressor adders and Sklansky adders are used for the realization of the novel low power and high speed Wallace tree multiplier [3]. In the low power and high speed multiplier architecture, 4:2 and 5:2 compressors are used for the partial product reduction in the second phase whereas Sklansky adders are used to perform addition in the final stage of the Wallace multiplier reduction.

In the partial product reduction stage, if the number of adders used are decreased, it correspondingly reduces the latency in the Wallace tree multiplier. Two full adders having delay of four units are replaced by a single 4:2 compressor having latency of three units and 5:2 compressors having latency of four units replace three full adders having latency of six units. The multiplexer blocks replace the XOR blocks in these compressors [4]. Therefore, in these compressors, the outputs generated at each stage are expeditiously used. In place of CMOS multiplexers having transistor count of twelve, transmission gate multiplexers (as shown in Figure 3) having transistor count 8 are used. The critical path delay is minimized because the select bits to the multiplexers are available much ahead of the inputs. 4:2 Compressor, 5:2 compressor and a carry generation module are shown in Figure 4, Figure 5, and Figure 6 respectively. Sklansky adders are chosen due to their lower power consumption and high speed of operation in contrast to other tree adders.

In comparison to the conventional Wallace tree multiplier, this low power and high speed Wallace multiplier as presented in Figure 7, has the advantage of reduced latency to 44.4% and also power reduction to 4.57% and 6.36% at an operating frequency of 50 MHz and 400 MHz respectively at 3.3V.

5. Booth Recoded Wallace Tree Multiplier

Booth Recoded Wallace Tree Multiplier comprises of Booth recoding algorithm and compressor adders for its realization [5]. In this architecture, Booth Recoding algorithm is introduced to generate and reduce the number of the partial products of multiplier, whereas, 3:2, 4:2, and 5:2 compressor structures are introduced to reduce the number of partial product addition stages (Figure 8). In these compressors, critical delay path is minimized by

replacing the XOR blocks with multiplexer blocks. Final two rows are summed using Carry Select Adder to produce the final result.

32x32 bit Booth Recoded Wallace tree multiplier has been compared with different types of multipliers as depicted in Table 2.

This architecture has the advantage of higher speed and lower area. It is 67% faster than the existing Wallace-tree multiplier, 22% faster than the radix-8 Booth multiplier, 53% faster than the Vedic multiplier, 16% faster than the default multiplier and 18% faster than the radix-16 Booth algorithm.

6. An Efficient High Speed Wallace Tree Multiplier

In contrast to the conventional Wallace tree multiplier, an efficient high speed Wallace tree multiplier is composed of compressor adders and modified carry select adder [6]. In this architecture, 4:2 and 5:2 compressors are used for partial product reduction in the second phase whereas carry select adders are used to perform addition of two rows of bits in the final stage for reduction in carry propagation latency of the Wallace multiplier.

Figure 9 shows the modified 16-bit carry select adder. Here, groups of 4 bits each are divided. In the modified 16-bit carry select adder, conventional RCA is used to add the least significant 4 bits, and others are added with incrementer in parallel. Then 10:5 multiplexer along with basic unit is used for calculating the final sum.

An efficient high speed Wallace tree multiplier architecture has the advantage of reduced latency which causes 44.4% higher speed, and 11% reduced power consumption than the conventional Wallace multiplier. Latency and number of transistors comparison is shown in Table 3. Area is also reduced in an efficient high speed Wallace tree multiplier than the conventional one.

7. Conclusion

In this paper, we have studied several types of Wallace tree multipliers and compared them to the conventional Wallace tree multiplier. In the reduced complexity Wallace tree multiplier, the number of half adders is reduced to 80 % with increase in number of full adders. Therefore, complexity is reduced contrary to the conventional Wallace multiplier.

In a novel low power and high speed Wallace tree multiplier, 44.4% faster speed whereas 4.57% and 6.36% of reduced power consumption at an operating frequency of 50 MHz and 400 MHz respectively at 3.3 V is achieved.

32x32 bit Booth recoded Wallace tree multiplier is 67% faster than the existing Wallace-tree multiplier, 22% faster than the radix-8 Booth multiplier, 53% faster than the Vedic multiplier, 16% faster than the default multiplier present in the Virtex 6 FPGA, and 18% faster than the radix-16 Booth algorithm. It is also area efficient.

An efficient high speed Wallace tree multiplier, speed is increased to 44.4 %, power consumption is reduced to 11 % and transistor count is reduced from 2998 to 2748. This multiplier shows best performance in comparison all the Wallace tree multipliers discussed in this paper, thus better viable option for future applications.

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Ms. Himanshu Bansal was born in Hanumangarh, Rajasthan, India on 23/05/1990. She has done B. Tech. in Electronics and Communication Engineering from the Faculty of Engineering and Technology, MITS, Rajasthan, India in 2012. Presently, she is pursuing M. Tech. in VLSI Design from the same university.

Dr. K. G. Sharma received B.E. degree in Electronics and Communication Engineering from Madan Mohan Malviya Engineering College, DDU University, Gorakhpur, completed his M Tech. degree in VLSI design from Faculty of Engineering & Technology, MITS and Ph.D in low power VLSI design from SGVU, Jaipur. He demonstrated his skills in R&D of Industrial Electronics, Kanpur for a briefer period and then he shifted to academics and shared his knowledge as lecturer at CSJM University, Kanpur in the initial stages of his career. He extended his profession as Faculty of Engineering and Technology in MITS from 2003 and with experience promoted to Asst. Professor in the same university. Because of his extensive research work, he has more than 50 research papers published in various international/ national journals and conferences. His current research interest comprises high speed and low power VLSI device designs.

Dr. Tripti Sharma earned B.E. degree in Electronics Engineering from North Maharashtra University, M Tech. degree in VLSI Design from Faculty of Engineering & Technology, MITS, RajasthanandPh.D in low power VLSI design from SGVU, Jaipur. After stepping into professional world, she started as lecturer with C.S.J.M University, Kanpur and continued it up to late 2003. After that she joined Faculty of Engineering & Technology, Mody Institute of Technology and Science, Rajasthan. Her working habits and discipline made her popular among the university and she was later awarded with designation of Asst. Professor in 2009. Her current research interests include digital VLSI circuits. She has over 40 papers published in International and national Journals and over 10 presentations in International and National Seminars / Symposia/ Conferences.
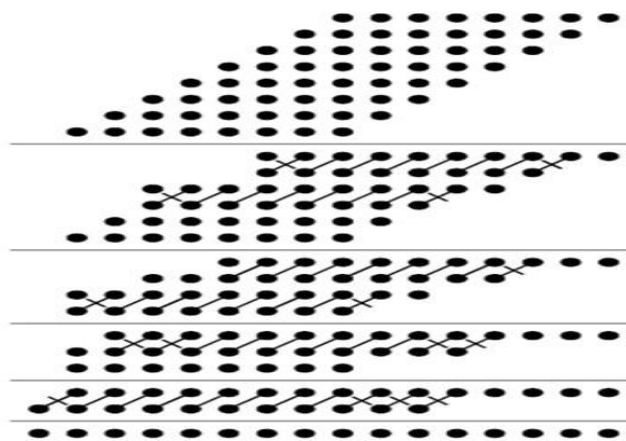

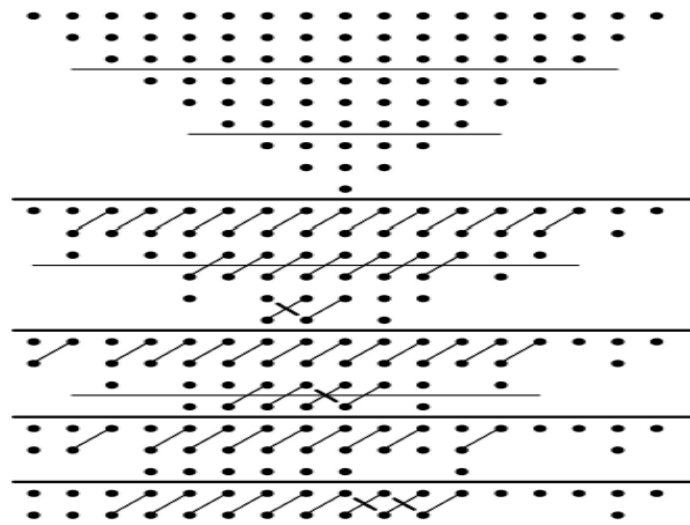Figure 1. Conventional 8-bit by 8-bit Wallace Reduction

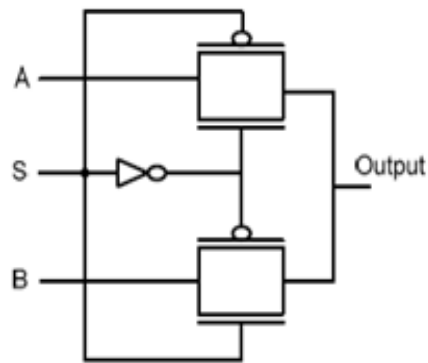Figure 2. Reduced Complexity Wallace 9-bit by 9-bit Reduction
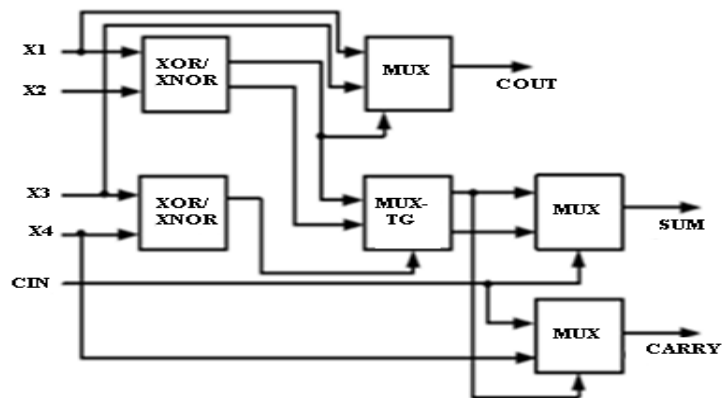

Figure 3. Transmission gate Multiplexer
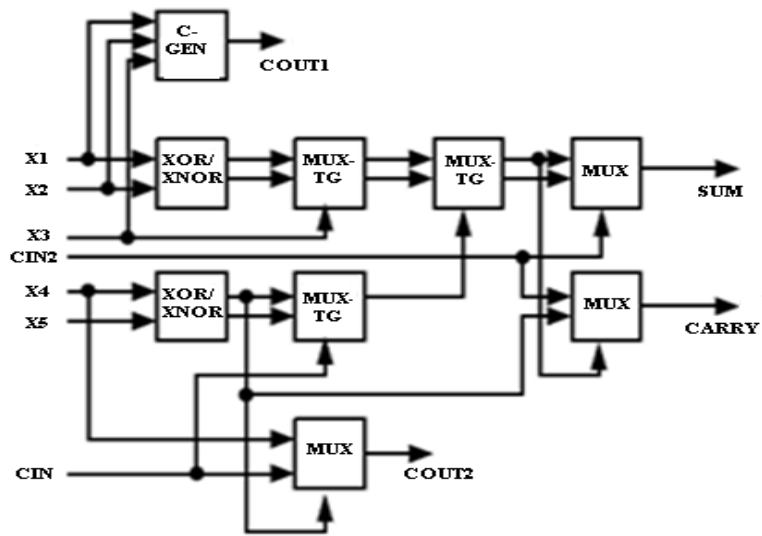

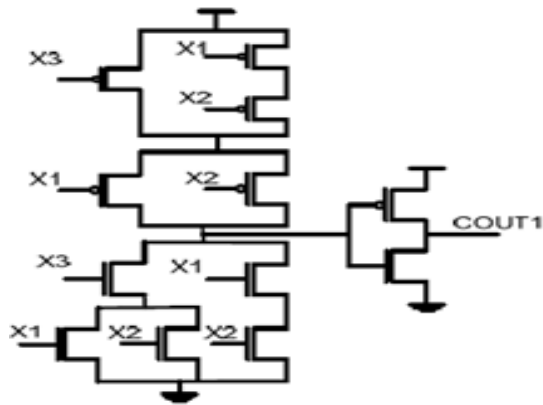Figure 4. A 4:2 Compressor

Figure 5. A 5:2 Compressor
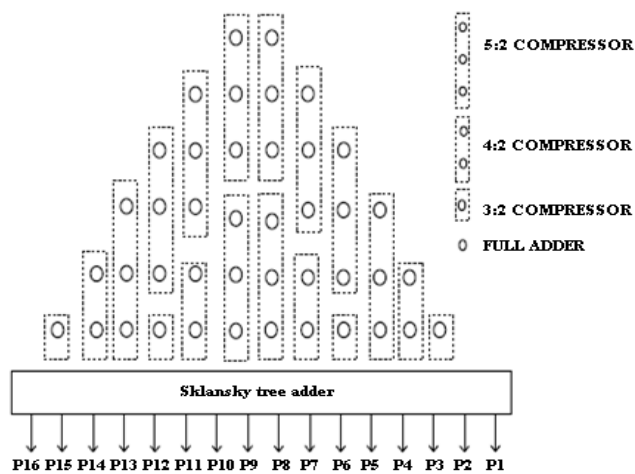

Figure 6. Carry generation module (C GEN)

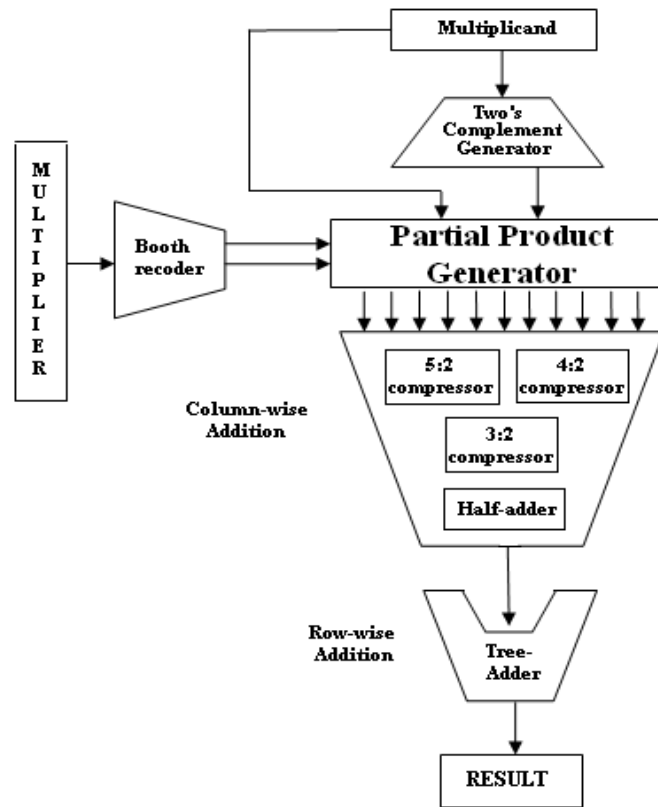Figure 7. A novel low power and high speed Wallace tree Multiplier

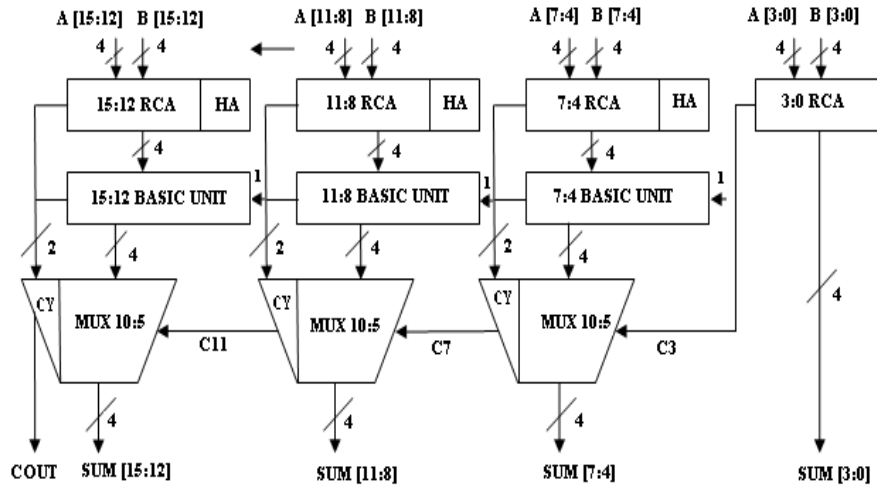Figure 8. Booth Recoded Wallace Tree Multiplier Architecture

Figure 9. Modified 16-bit Carry Select Adder structure

Table 1. Complexity of the Reduction (Second Phase)

Input Size (N)	8	16	24	32	64
Stages (S)	4	6	7	8	10
WALLACE					
Full Adders	38	200	488	96	3850
Half Adders	15	52	100	156	430
Total Gates	402	2008	4801	8778	36388
MODIFIED WALLACE					
Full Adders	39	201	490	907	3853
Half Adders	3	9	16	23	53
Total Gates	363	1845	4474	8263	34889

Table 2. Delay Comparison

Types of Multiplier	Width	Delay (ns)
Wallace Tree Multiplier	8-bit	7.168
Multiplier using Vedic mathematics	16-bit	13.452
Modified-Booth Multiplier (Radix-8)	32-bit	12.081
Modified-Booth Multiplier (Radix-16)	32-bit	11.564
XC6vlx75tl-1Lff484 FPGA Default Multiplier	32-bit	11.238
Booth Recoded Wallace Tree Multiplier	32-bit	9.536

Table 3. Number of Transistors (N) and Latency (L) Comparison

	Wallace Tree Multiplier	
	N	L
Conventional Wallace Multiplier	2998	27
An Efficient High Speed Wallace Tree Multiplier	2748	15

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