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Low Power &High Speed Domino XOR Cell

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Abstract

The XOR gate plays an important role in digital system like arithmetic circuits and encryption circuits. This paper proposes a domino XOR cell designed using hybrid domino logic technique. The proposed design demonstrates better power consumption, better delay and hence better power delay product (PDP) at varying supply voltages, frequency and temperature when compared with existing design along with full voltage swing. All simulations are performed on 90nm standard model on Tanner EDA tool version 13.0.

Keywords: Domino, low power, PDP and XOR.

1. Introduction

In complex digital implementations where increasing speed and reduction of silicon area is the major objective, domino logic circuits give many significant advantages over static logic circuits [1]. Thus, domino circuits can be used to realize many complex and wide fan in logic function such as wide OR, AND, XOR, XNOR gates due to high speed and low area characteristics of domino CMOS circuits. It allows a significant reduction in the number of transistors required to realize a function than CMOS technology. This technique is faster than other similar logic families such as static logic, DCVSL and PTL [2] [3].It does two operations, precharging the output node capacitance and subsequently, evaluating the output level according to the applied inputs. Both of these operations are scheduled by a single clock.

XOR gate is one of the arithmetic units used in various VLSI applications such as adder, subtractor, comparator, multipliers and parity generator etc. [4-7]. The performance of whole arithmetic circuit is affected by the individual performance of XOR cell, therefore for improving the performance of whole system, enhancing the performance of XOR cell is most important [8] [9].

This paper proposes a domino XOR circuit which increases the output voltage swing significantly as compared to existing design and improves the power consumption too. The paper is organized as follows: Section 2 describes previous work as reported in the literature. Section 3introduces the proposed domino XOR cell. Simulation results and their comparisons are included in Section 4 and finally Section 5 concluded the paper.

2. Previous work

The schematic of hybrid domino XOR gate is shown in Fig.1. It adopts both N and P type transistors in the pull-down network. In this circuit, two series combination paths of N and P type transistors are connected in parallel. Transistor N4 is connected in series to footer transistor N3. To increase the speed, a current mirror circuitry is also added in pull down network [10]. (Note 1)

However, for input combinations 01 or vice-versa, the circuit gives 0 or logic low at output node instead of giving 1 or logic high. This happens because no conducting path occurs between dynamic node V1 and ground for this input combination. Table I depicts the measured output levels of this design.

3. Proposed domino XOR Cell

The schematic of proposed domino XOR cell is shown in Fig. 2. This circuit overcomes the problems occurred in existing XOR cell. The source terminal of pMOS transistor P1 and drain terminal of nMOS transistor N1 are connected to V_{DD}. The transistor P1 is used as precharge transistor while N4 is used as footer transistor. Single

clock signal is used to drive both of these transistors in each dynamic stage. Instead of connecting pMOS as keeper transistor, nMOS transistor N1 is connected in parallel with transistor P1 so that inverting functions can also be implemented in domino design techniques. This eliminates the need of another inverter for generating inverted functions [1]. And thus, both XOR and XNOR gates can be implemented in single design. Two nMOS transistors N6 and N7 are also added to obtain correct output for combinations AB=11. The current mirror connected in Fig. 1 has been removed as this part was only consuming area and in turn gives increased power consumption of the design. (Note 2)

The circuit operation takes place in two phases i.e. precharge phase and evaluation phase. In precharge phase, clock signal is low. P1 will turn on. Footer transistor N4 is turn off. Dynamic node V1 is charged to high voltage by pull up transistor. Now keeper transistor N1 will turn on to keep dynamic node at high voltage level and overcome charge sharing effect. In precharge phase input signal will not affect the output. There is no discharging path between dynamic node and ground. Therefore we get low voltage at output node. Table I depicts the performance of both existing and proposed designs. From the table it is clear that proposed circuitry has shown improved threshold loss and verifies the logical expression of XOR gate as compared to existing one.

In evaluation phase, clock signal is high, the pull-up transistor P1 and N1 will turn off and footer transistor N4 will turn on. This phase is further divided in four cases. Here, charging or discharging of the dynamic node is depending upon input signals.

Case 1: When both input signals are low i.e. A=B=0, P2 and P3 turn on in pull down network and rest will be in off state. There is no conducting path between dynamic node and ground to discharge the dynamic node voltage. So, it will remain at high logic. Therefore, get low logic at output.

Case 2: When both input signals are at different logic state, i.e. A=0 and B=1, it will turn on the series connection of transistor N3 and P3 of pull down network. Now there will be a conducting path between V_{DD} and ground. This will discharge the dynamic node and get high logic at the output node.

Case 3: When A=1 and B=0, it will turn on the series connection of transistor N2 and P2 of pull down network. Now again there will be a conducting path between V_{DD} and ground. This will discharge the dynamic node and get high logic at the output node.

Case 4: When both input signals are high, i.e. A=B=1, N2, N3 will turn on and P2, P3 will turn off in pull down network and N6 and N7 turn on. These two transistors become active only for this state. They will provide high voltage at dynamic node to verify the function of the XNOR and XOR gate. Thus, we get high logic at dynamic node and low logic at output node.

4. Simulation and Comparison

All simulations are performed on Tanner EDA tool version 13.0 using 90nm technology [11] with input and supply voltage ranging from 0.5 V to 1.0 V in steps of 0.1 V. In order to prove that proposed design is consuming less power, delay and have better performance, simulations are carried out for power consumption at varying input voltage, temperature and frequency.
The graph shown in Fig. 3 reveals that the power-delay product (PDP) of proposed design is remarkably less than existing design. The current mirror circuitry in existing design remains always ON in evaluation phase so it consumes more power than proposed design. (Note 3)

Fig. 4 shows that overall PDP of proposed design is lesser than the existing design with varying temperature. As temperature increases it increases thermal generation of majority and minority carries and also increases recombination rate and hence the characteristics of semiconductor device are affected [12]. (Note 4)

The graph in Fig. 5 shows that the PDP of proposed design is better than existing design. (Note 5)

5. Conclusion

The proposed domino XOR gate outperforms the existing design in terms of PDP with varying input voltage, operating frequency and temperature. It also gives much better output voltage swing with comparison to its peer design. Hence, this new design is a viable option for low power complex system design.

References

S. Kang and Y. Leblebici, (2003), “CMOS Digital Integrated Circuits, Analysis and Design”, (3rd ed.). Tata McGraw-Hill. (Chapter 6 and Chapter 9)

M. Kishor and J. P. D. Gyvez, (2000), “Threshold Voltage and Power-Supply Tolerance of CMOS Logic Design

Families", *IEEE Proc. DFT'00*, pp. 349-357.

V. Kursun and E. Friedman, (2003), "Domino logic with variable threshold voltage keeper", *IEEE Trans on VLSI Syst.*, vol. 11, no. 6, pp. 1080 -1093.

M. N Senejani, M. Hosseinghadiry, Miryahyaei, (2009), "Low Dynamic Power High Performance Adder", ***International Conference on*** *Future Computer and Communication (ICFCC),*pp. 482-486.

Wang. J, Gong. N, Hou. L, Peng. X, Geng. S and Wu. W, (2011), "Low power and high performance dynamic CMOS XOR/XNOR gate design", *Microelectronics Engineering*, vol.88, pp.2781-2784.

Chip-Hong Chang , JiangminGu , Mingyan Zhang, (2004), "Ultra low-voltage low-power CMOS 4-2 and 5-2 compressors for fast arithmetic circuits", *IEEE Transactions on Circuits and Systems*, vol. 51, pp. 1985-1997.

S. Singh, T. Sharma, K. G. Sharma, B. P. Singh, (2012), "Array Multiplier using pMOS based 3T XOR Cell", *Innovative Systems Design and Engineering*, vol. 3, no 5.

A. Bellaouar and Mohamed I. Elmasry, (2012), "Low-power Digital VLSI Design: Circuits and Systems", (3rd ed.), Kluwer Academic Publishers. (Chapter 2)

N. Weste and K. Eshraghian, (2010), Principles of CMOS VLSI Design: A System Perspective, (3rd ed.), Addison-Wesley. (Chapter 4 and Chapter 5)

A. K. Pandey, J. K. Tiwari, R. A. Mishra, R. K. Nagaria, M. Tiwari, (2013), "Design of New Low Leakage Power domino XOR Circuit", *International Journal of Computer Applications (0975 – 8887)*, vol. 65, no. 1, pp. 28-32.

PTM, http://www.eas.asu.edu/~ptm.

Socher E, Beer S M and Nemirovsky Y, (2005), "Temperature sensitivity of SOI-CMOS transistors for use in uncooled thermal sensing", *IEEE Trans. Electron Devices*, vol. 52, no. 12, pp. 2784-2790.

Notes

Note 1. This is Hybrid domino XOR cell.

Note 2. This is proposed domino XOR cell.

Note 3. This is graph of PDP with increasing input voltages.

Note 4. This is graph of PDP with increasing temperature.

Note 5. This is graph of PDP with increasing frequency.

Table 1. Performance table of existing and proposed domino XOR cell.

Clock	A (Volt)	B (Volt)	Expected Output (Volt)	Obtained Output (Volt)	
				Existing	Proposed
0	0	0	0	0.003	0.01
0	0	1	0	0.015	0.01
0	1	0	0	0.015	0.01
0	1	1	0	0.020	0.01
1	0	0	0	0.025	0.01
1	0	1	1	0.255	0.95
1	1	0	1	0.256	0.96
1	1	1	0	0.015	0.010

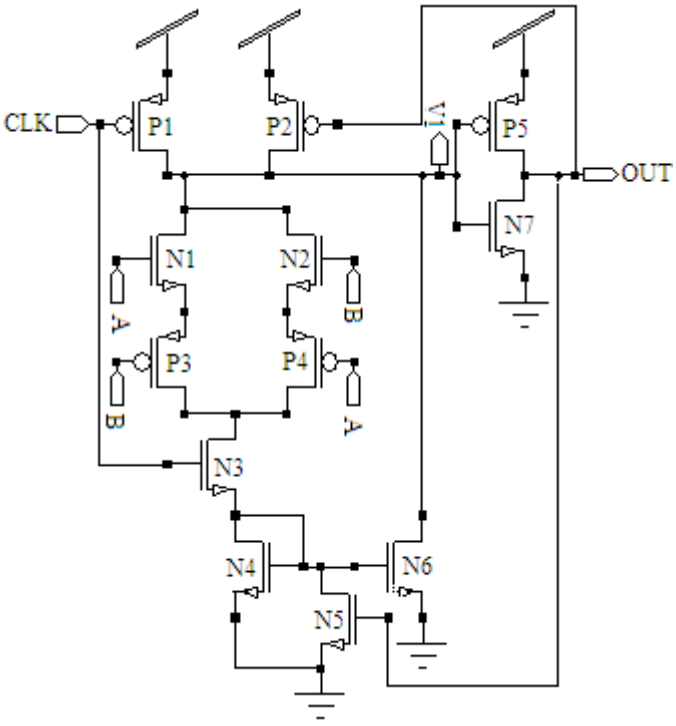

Figure 1. Hybrid domino XOR cell.

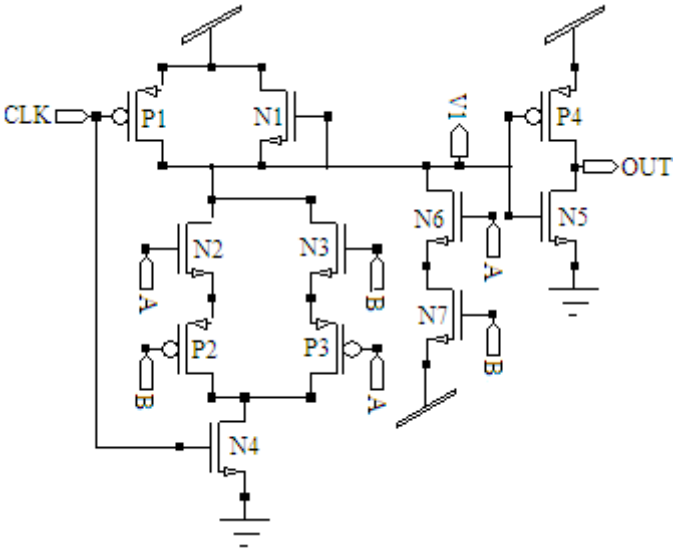

Figure 2. Proposed domino XOR cell.

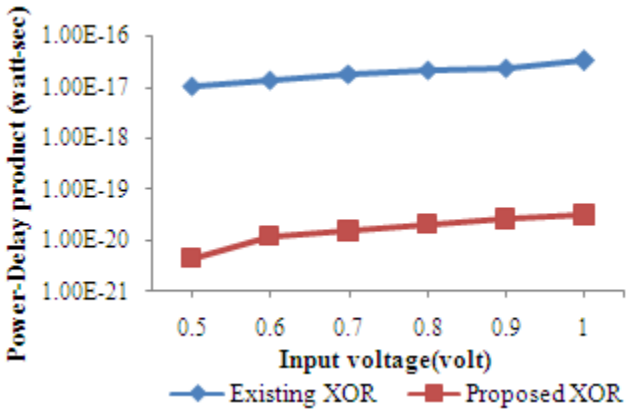

Figure 3. Power-Delay Product with increasing input voltage.

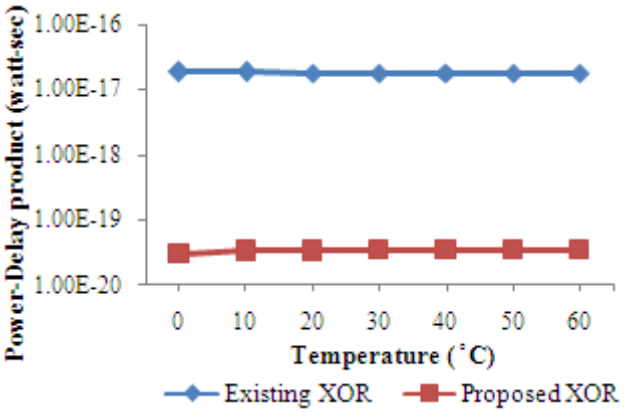

Figure 4. Power-Delay Product with increasing temperature.

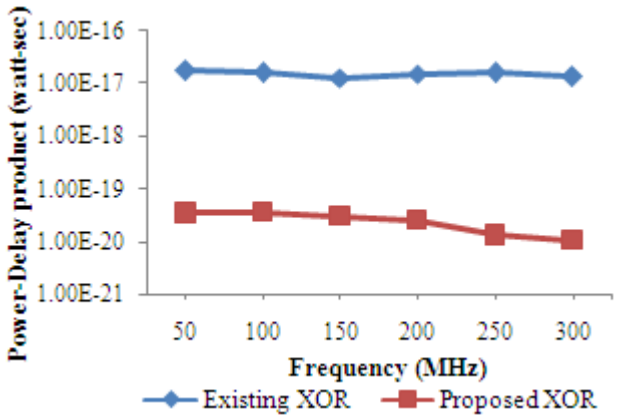

Figure 5. Power-Delay Product with increasing frequency.

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