Innovative Systems Design and Engineering
ISSN 2222-1727 (Paper) ISSN 2222-2871 (Online)
Vol.6, No.9, 2015

Design Optimization of Double Gate Based Full Adder

Mohit Chopra
Department Of Computer Science, DAV College, Jalandhar Punjab, India

Prof. Navneet Gill, Dr. Harjeet Singh
Department of E C E, CTIEMT, Shahpur Jalandhar, India

Abstract
Full adder is the essential block of circuit of arithmetic's found in microprocessor and microcontroller in ALU (arithmetic and logic unit). Improving the performance of the adder is very important for up gradation the performance of digital circuit of electronics in which adder is utilized. The main aim of designing of arithmetic circuit is the power consumption. In an arithmetic circuit, the adder is a critical module for operation of addition and also the core for many operations related to arithmetic. Therefore it is obliged to decrease the consumption of power of adder circuit so as to diminish the consumption of the module related to arithmetic. In this paper, a review of double gate based full adder is presented. Various works on this research work which is already available is presented and also problem related to them are presented.
Keywords: DG-MOSFET, ALU, XOR, Full Adder,PTI, GDI, Diffused Gdi,Finfet, ELK, Power Grating , Stacking .

1. Introduction

There are number of circuits of full adder has been designed owing to its significance in various electronic circuits. The full adder circuit is core of many digital and analog circuits. It is used as major Fiureuring circuits for mainly digital designs. The full adder circuit is analyzed for low power, reduced delay, and low power delay products. The progress in the field of portable systems and cellular networks has increased the research efforts in low power microelectronics. The design criterion of a full adder cell is usually multi-fold. Transistor count is a primary concern which largely affects the design complexity of many function units such as multiplier and algorithmic logic unit (ALU). The limited power supply capability of present battery has made power consumption an important Figureure in portable devices. The speed of the design is restricted by size of the transistors, parasitic capacitance and delay in the critical path. If the full adders lack driving capability then it requires additional buffer, which consequently increases the power dissipation. In the last decade, the full adder has gone through substantial improvement in power consumption, speed and size, but at the cost of weak driving capability and reduced voltage swing. However, reduced voltage swing has the advantage of lower power consumption,[S. Verma, D. Kumar, G.K. Marwah(November 2014)] [Manisha, , (June 2014.)].

[Soolmaz Abbasalizadeh and Behjat Forouzandeh (june 2014)] proposed 1-bit full adder using double-gate FinFet transistor and Gate Diffusion Input (GDI) technique. Using GDI cell makes it possible to reduce the number of transistors and merging this technique with double gate process causes further reduction in power and delay. In this paper, method of using double gate transistor in logic circuits and its benefits are presented. 1 bit full adder with this transistor and using GDI (Gate Diffusion Input) technique is simulated in 45nm double gate FinFet model and compared with previous works. The results show that, this full adder has lowest power and power*delay among other works in MHz operational frequency. By using GDI cell and double gate transistor, this full adder exhibits lower power*delay and average power compared with the others.

[Jayram Shrivas , Shyam Akashe and Nitesh Tiwari in(may,2012)] implement a reliable and energy efficient full adder circuit cell. In this paper, they develop a consistent and energy proficient new adder cell has 11 transistors, and it is based on the low power designs for the GDI presented in and on transmission gates and pass-transistors. In this paper, The GDI (gate diffusion input) technique has been used for simultaneous generation of XOR gate. The main idea behind the designing of this 11 transistors full adder to improve the performance of 10 transistors full adder design mentioned in literature by sacrificing a transistor count. While the proposed full adder has negligible area overhead, it has improved the power consumption of the circuit when compared with the 10T full adder circuit. The GDI cell shown in Figure.2 was proposed by [Morgenshtein et. al.(2013)]. It is design which is very flexible for digital circuits. This technique optimizes the power dissipation and also reduces transistor count. The advantage of GDI technique two-transistor implementation of complex logic functions and in-cell swing restoration under certain operating conditions, are unique within existing low-power design techniques. XOR gate using GDI (gate diffusion input) technique is shown in Figureure.3. The performance of the proposed 11T full adder circuit has been shown to outperform the 10T full adder, which can operate at low-voltages and have good output swings. At the cost of negligible area overhead power consumption of 11t adder circuit is decreased approx. 42.47% at varying supply voltages. Hence the proposed design can be suitable for low power application. First, as we CONCLUDED from the Figures, for any input

combination there can never be a direct path from the power supply to the ground, this implies that there is no short circuit current. This circuit gives low power but again outputs are degraded. The delay of circuit is higher due carry generating part.

[Richa Saraswat, Shyam Akashe and Shyam Babu in (2015)] provide a flexible and reliable finfet based full adder circuit. Double Gate FINFET has two electrically independent gates, which gives circuit designer more flexibility in design low-power and efficient gates. Double Gate Field Effect Transistors have been indicated as alternatives to reduce the Short Channel Effects (SCE) of scaled devices due to their better electrostatic control of channel charges. In this paper, they propose a low power and area efficient full adder. The basic advantage of 10 transistors full adders are-low area compared to higher gate count full adders, lower power consumption, and lower operating voltage. It becomes more and more difficult and even obsolete to keep full voltage move backward and forward operation as the designs with fewer transistor count and lower power consumption are pursued. The reduction in voltage swing, on one hand, is beneficial to power consumption. On the other hand, this may lead to slow switching in the case of cascaded operation such as ripple carry adder. So there is no problem of degraded output.

This paper proposes a -Bit full adder cell using Double Gate FINFET (Fin Shaped Field Effect Transistor) at 45nm CMOS technology. The intention of this paper is to reduce leakage power and leakage current of 1-bit Full Adder while maintaining the competitive performance with few transistors are used (transistors count i_0) Double Gate FINFET technique which decreases the process variation on 1-bit Full Adder is presented in this paper; the key of Double Gate FINFET technique is applied on 1-bit Full Adder is to reduce the operating power, leakage power and leakage current. We investigate the use of Double Gate FINFET technology provides low leakage and high performance operation by utilizing high speed and low thresh hold voltage transistors for logic cells. Which show that it is particularly effective in sub threshold circuits and can eliminate performance variations with Low power. Digital CMOS circuit may have three major sources of power dissipation namely dynamic, short and leakage power. Hence the total power consumed by every MUX style. Thus for low-power design the important task is to minimize C L, V dd, Vf , elk while retaining required functionality. The first term Pdyn represents the switching component of power, the next component Psc is the short circuit power and Pleak is the leakage power. Where, CL is the loading capacitance, fClk is the clock frequency which is actually the probability of logic 0 to 1 transition occurs (the activity factor). Vdd is the supply voltage, V is the output voltage swing which is equal to V dd. A 1-Bit Full Adder based on DG FINFET technique have been proposed. The analysis of the simulated results confirms the feasibility of the DGFINFET technique in full adder design and shows that there is reduction of 25 to 30 percent in the value of power dissipation parameter as compared to CMOS technique at supply voltage of 0.7V. DG FINFET adders have a marginal increase in area compared to the CMOS adders.

[Shyam Akashe and Anuj Kumar Shrivastava (2014)] proposed 1 bit full adder, In this paper we designed full adder with the help of double gate transistor, the used parameters value has been varied significantly thus improving the performance of full adder. Power Gating is one of the most used circuit techniques to reduce the leakage current in idle circuit. In this paper different parameters are analysed on Power Gating Technique. Simulation results of double gate full adder have been performed on cadence virtuoso with 45nm technology.

Full adder is a combinational circuit that performs the addition operation of input bits. Full adder basically consists of three inputs and two outputs. The input variables are dented by A, B and Cin. The two output variables are denoted by sum(S) and carry (Cout). Figure. 5 shows the basic block diagram of full adder cell. The Boolean expression for full adder operation is

Figure. 5 shows the double gate 10T full adder circuit. This adder circuit is constructed by using the 4T XOR gate. XOR gate is the basic element of full adder cell and generates the basic addition operation of adder cell. It behaves like a single half adder cell. Conventionally XOR gate use 8 MOSFETs for proper working, topologies. Here we have used 4T XOR gate to increase circuit density. The 4T XOR gate. Reduction in size of full adder is achieved by using this XOR gate and overall leakage is also reduced.

3. Power gating technique

Power Gating, it reduces the leakage by inserting n- MOS and p-MOS to the circuit. Figure. 6 shows the Power Gating circuit. This technique is very widespread for reducing leakage in the circuits. Because of the easiness of execution of the technique, power Gating has been used to minimize leakage energy in circuits at the architectural level [8 Pankaj Kumar, Poonam Yadav(March 2014)]. [9 J.K. Sahani, S. Singh, (February 2015)]. The effectiveness of power gating required following:

- It provides the switches for turning off and on of the functional units at circuit level.
- These switches controls the power gate at various parts of the circuit can be provided as handles at the system software or the level thereby giving the system compiler the ability to control them.

4. Problem Formulation

In the above section, research work which is already done on full adder is presented. But the full adders which are available have some problems which we will be taking care in our work. The problems are given below. The existing circuit consists of more number of transistors. The power dissipation as well as power delay of product is higher. There are degradations in output results for carry and sum module.

5. Simulation results for base circuit

The simulations are done using SPICE tool in a 45 nanometer (*nm*) standard CMOS technology at room temperature; with supply voltage of 0.7 at 100 MHz frequency. The input and output waveforms show that this circuit works perfectly as full adder circuit and have very less degradation in outputs of this circuit. The waveforms are shown in Figure.7. The simulations shows a following results for power consumption and delay.

5.1 *Power Results*

Average power consumed-> 1.254695e-007, power delay product is $784\times e^{18}$ and power supply is 0.7.

6. New Technique

6.1 Methodology

To understand concept of full adder and its usability in electronic circuit designing. To understand techniques used to improve parameters of proposed FULL adder. We have proposed an improved 1-bit full adder circuit which consumes low power and gives faster response for output. The proposed adder circuit consists of 10-transistors and called as 10-T adder cell. The proposed circuit is implemented using three main components, namely XOR, inverter, and Multiplexer. To reduce the leakage current in the circuit, a stack pMOS transistor is added into one of the inverter. The proposed circuit is simulated for total power consumption and delay. When the inputs A=B=0, the XOR gate will introduce 1-Vt loss and this loss causes the nMOS transistor (N1) of the inverter not to be completely turned off (weak inversion) and results in subthreshold leakage current. The subthreshold leakage current causes higher power dissipation in the circuit. To avoid this leakage current problem, we have introduced a pMOS (P-stack) transistor in series with the pull up transistor of the inverter. This extra transistor gives lower leakage as well as ensures that pull up pMOS is completely off when either inputs (A or B) are high. The added transistor will slightly degrades the response of carry-out because pMOS is slower device.

6.2. Stack Effect

Subthreshold current depends exponentially on VT, VDS and VGS. Therefore it is a function of the terminal voltages, VD, VB, VS and VG. This means that to know subthreshold leakage of a device the biasing condition should be known or by controlling the terminal voltages the subthreshold leakage can be controlled. Input pattern of each gate affects the subthreshold as well as gate leakage current. The leakage of transistors in a stack is a function of no. of transistors and input pattern. Source biasing is the general term for several techniques that change the voltage at the source of a transistor.

Figure.8 Stack of 3 NMOS transistors M1, M2 and M3.The goal is to reduce VGS, which has the effect of exponentially reducing the subthreshold current. Another result of raising the source is that it also reduces VBS, resulting in a slightly higher threshold voltage due to the body effect. Circuits that directly manipulate the source voltage are rare, and those that exist usually use switched source impedance or a self-reversed biasing technique Theoretically, the source voltage of the upper transistor will be a little higher than the source voltage of the lower transistors in the stack. Hence VGS of upper transistor is negative, VBS is negative resulting in increase in threshold voltage and VDS is also lower. Due to this, the leakage of upper transistor reduces. This reduction is called stack effect.

7. Conclusion

In this paper, a review of the various works on the full adder which is based on double gate has been done. For the performance analysis of numerous full adders, distinct parameters are measured such as number of transistors utilized, power dissipation, power delay product of circuit and delay. The various works done on the full adder are presented in this paper are studied. The modified GDI full adder shows low power dissipation as compare to GDI full adder. The finFET based full circuit is shows low power and works at low power supply. The power gating technique shows increased number of transistors. To overcome these problems, technique called stacking will be used in proposed work.

Acknowledgment

The paper has been written with the kind assistance, guidance and active support of my Guide Ms. Navneet Kaur and Co-Guide Dr.Harjeet Singh and my HOD Prof. Nischay Bhal who have helped me in this work. I would like

to thank all the individuals whose encouragement and support has made the completion of this work possible.

References

S. Verma, D. Kumar, G.K. Marwah, "New High Performance 1-Bit Full Adder Using Domino Logic", International Conference on Computational Intelligence and Communications Networks (CICN), pp 961-965, November 2014

Manisha, Archana "A Comparative Study of Full Adder using Static CMOS Logic Style", International Journal of Research in Engineering and Technology, Vol. 3, Issue 6, June 2014.

Soolmaz Abbasalizadeh, Behjat Forouzandeh "Full adder design with GDI cell and independent double gate transistor", 20th Iranian Conference on Electrical Engineering (ICEE), pp 130-134, 15-17 May 2012.

Jayram Shrivas, Shyam Akashe, Nitesh Tiwari, "Design and Performance Analysis of 1 bit full adder using GDI technique in nanometer era", World Congress on Information and Communication Technologies (WICT), pp.822-825, November 2012.

A. Morgenshtein, A. Fish, I.A. Wanger, "Gate-diffusion input (GDI)- a technique for low power design of digital circuits: analysis and characterization", IEEE International Symposium on Circuits and Systems (ISCAS), I-477 – I-480, Vol. 1, 2002.

Richa Saraswat, Shyam Akshe, Shyam Babu, "Designing and Simulation of full adder cell using FINFET technique", 7th International Conference on Intelligent Systems and Control (ISCO), pp. 261-264, 2013.

A.K. Srivaatava, Shyam Akshe, "Design high performance and low power 10T full adder cell using double gate MOSFET at 45nm technology", International Conference on Control Computing Communication & Materials (ICCCCM), pp 1-5, August 2013.

A.Pathak, S. Akashe, "A novel power gating technique for 3-bit flash analog to digital converter", 2nd International Conference o Signal Processing and Integrated Networks (SPIN), pp. 897-901, February 2015.

C. Shravan, C.P. Kumar, K. Sivani, "A novel approach for power-gating technique with Improved Efficient Charge Recover Logic", International Conference on Smart Electric Grid (ISEG), September 2014.

Pankaj Kumar, Poonam Yadav, "Design and Analysis of GDI Based Full Adder Circuit for Low Power Applications", International Journal of Engineering Research and Applications, Vol 4, Issue 3, pp 462-465, March 2014.

J.K. Sahani, S. Singh, "Design of Full Adder Circuit Using Double Gate MOSFET", Fifth International Conference on Advanced Computing & Communication Technologies (ACCT), pp 57-60, February 2015.

Lee Hanho, G.E. Sobelman, "A new low-voltage full adder circuit", Proceedings Seventh Great Lakes Sympsium on VLSI, March 1997.

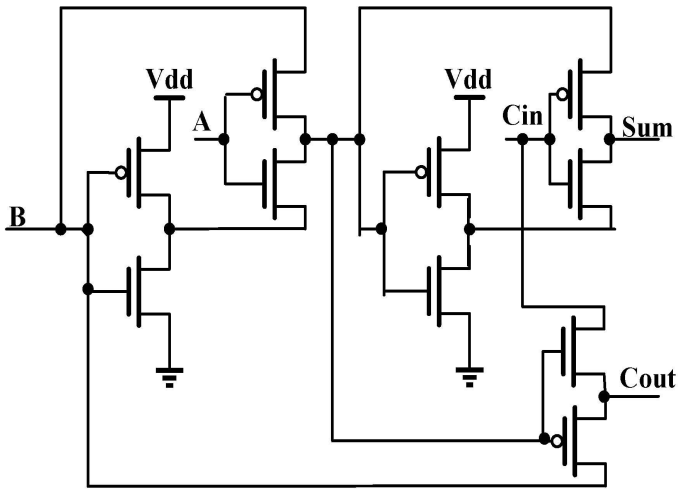

Figure. 1 GDI full adder

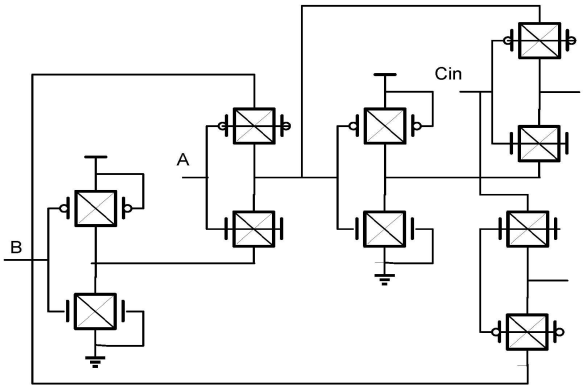

Figure. 2 GDI full adder with Double Gate

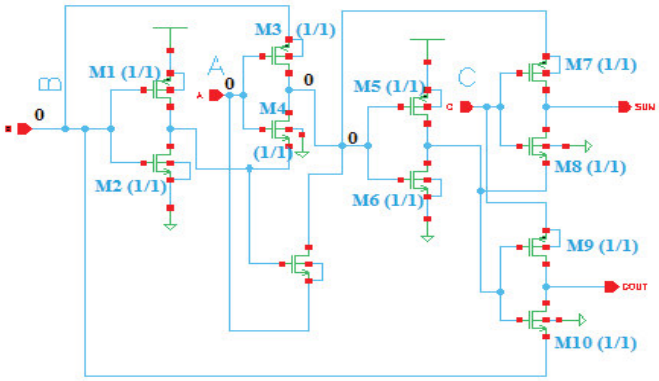

Figure. 3 Modified GDI based 11T full adder

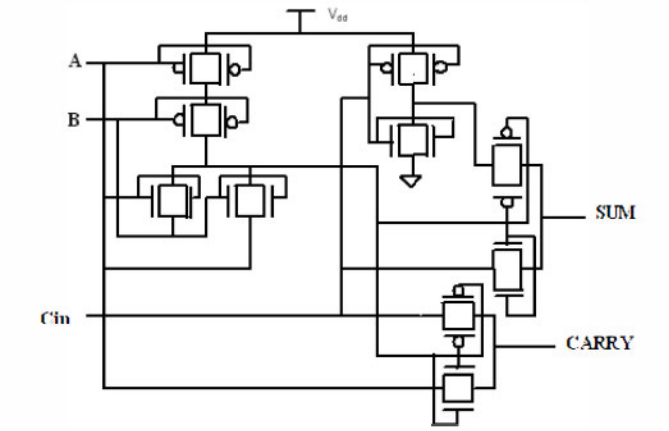

Figure. 4 Schematic of 1-bit full adder using FINFET

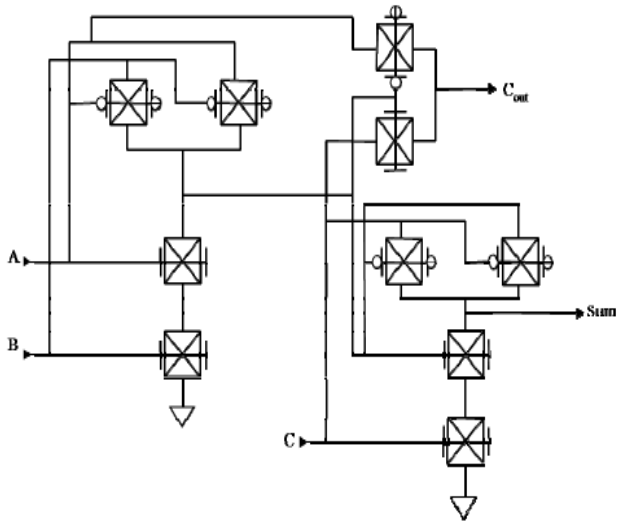

Figure. 5 Double Gate Full adder

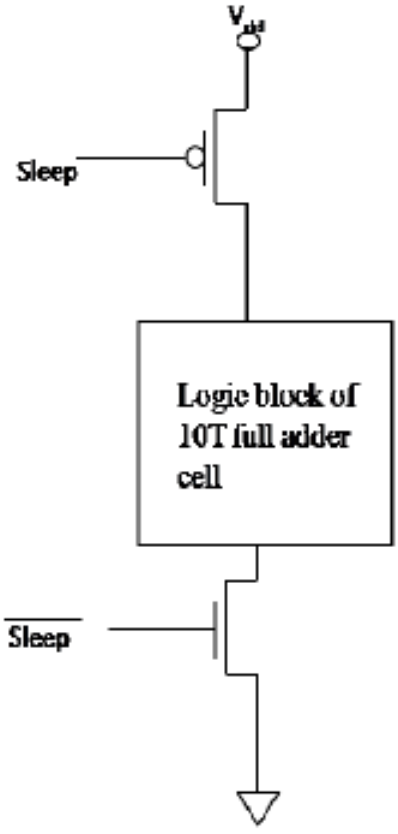

Figure. 6 power gating technique

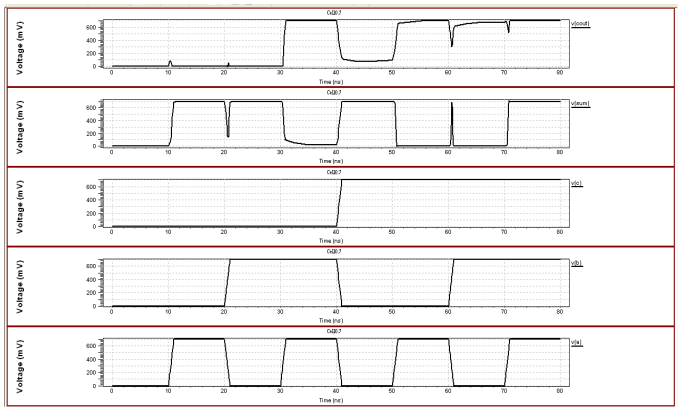

Figure.7 Input and Output waveform

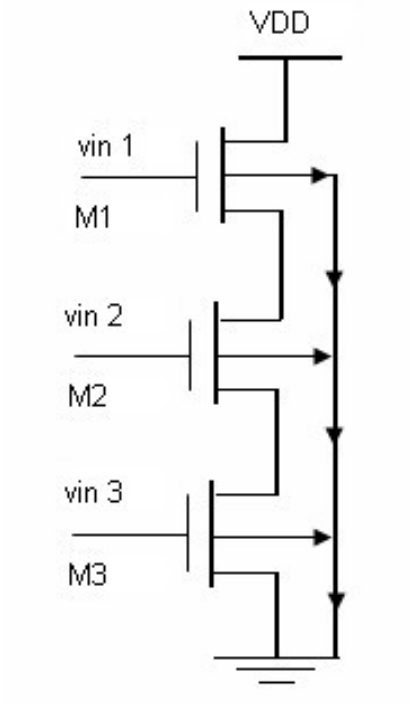

Figure.8 stack effect

The IISTE is a pioneer in the Open-Access hosting service and academic event management. The aim of the firm is Accelerating Global Knowledge Sharing.

More information about the firm can be found on the homepage:
http://www.iiste.org

CALL FOR JOURNAL PAPERS

There are more than 30 peer-reviewed academic journals hosted under the hosting platform.

Prospective authors of journals can find the submission instruction on the following page: http://www.iiste.org/journals/ All the journals articles are available online to the readers all over the world without financial, legal, or technical barriers other than those inseparable from gaining access to the internet itself. Paper version of the journals is also available upon request of readers and authors.

MORE RESOURCES

Book publication information: http://www.iiste.org/book/

Academic conference: http://www.iiste.org/conference/upcoming-conferences-call-for-paper/

IISTE Knowledge Sharing Partners

EBSCO, Index Copernicus, Ulrich's Periodicals Directory, JournalTOCS, PKP Open Archives Harvester, Bielefeld Academic Search Engine, Elektronische Zeitschriftenbibliothek EZB, Open J-Gate, OCLC WorldCat, Universe Digtial Library , NewJour, Google Scholar