Innovative Systems Design and Engineering www.iiste.org
ISSN 2222-1727 (Paper) ISSN 2222-2871 (Online)
Vol 2, No 4, 2011

Optimized SVPWM for Multilevel Inverter

Bandaru Urmila
G.. Pulla Reddy Engineering College, Kurnool
A.P., India
E-mail: urmila913@gmail.com

D. Subbarayudu
Brindavan Institute of Technology, Kurnool
A.P., India
E-mail: dsr@gmail.com

The research is financed by Asian Development Bank. No. 2006-A171(Sponsoring information)

Abstract
Multilevel inverters have gained interest in recent years in high-power medium-voltage industry. This paper considered the most popular structure among the transformer-less voltage source multilevel inverters, the diode-clamped converter based on the neutral point converter. This paper proposes a single carrier multi-modulation SVPWM technique with an optimized space vector switching sequence. Simulation results presents comparison of single and multicarrier optimized space vector switching sequence with general switching sequence of nine-level diode-clamped inverter for the parameter total harmonic distortion and fundamental component of voltage.

Keywords- Multilevel inverter, SVPWM, total harmonic distortion, Diode-clamped inverter, SCMMGS, MCMMGS, SCMMOS, MCMMOS

1. Introduction

Multilevel inverters have drawn tremendous interest in high-power medium-voltage industry. In literature, inverters with voltage levels three or more referred as multilevel inverters. The inherent multilevel structure increase the power rating in which device voltage stresses are controlled without requiring higher ratings on individual devices. They present a new set of features that suits well for use in static reactive power compensation, drives and active power filters. Multilevel voltage source inverter allows reaching high voltages with low harmonics without use of series connected synchronized switching devices or transformers. As the number of voltage levels increases, the harmonic content of output voltage waveform decreases significantly. The advantages of multilevel inverter are good power quality, low switching losses, reduced output dv/dt and high voltage capability. Increasing the number of voltage levels in the inverter increases the power rating. The three main topologies of multilevel inverters are the Diode clamped inverter, Flying capacitor inverter, and the Cascaded H-bridge inverter by Nabae et al. (1981). The PWM schemes of multilevel inverters are Multilevel Sin-Triangle Pulse Width Modulation-SPWM and Space Vector Pulse Width Modulation-SVPWM. Multilevel Sin-Triangle PWM involves comparison of reference signal with a number of level shifted carriers to generate the PWM signal. SVPWM involves synthesizing the reference voltage space vector by switching among the nearest voltage space vectors. SVPWM is considered a better technique of PWM owing to its advantages (i) improved fundamental output voltage (ii) reduced harmonic distortion (iii) easier implementation in microcontrollers and Digital Signal Processor. This paper considered the most popular structure among the transformer-less voltage source multilevel inverters, the diode-clamped converter based on the neutral point converter proposed by Carrara et al.(1992) with SVPWM technique. This paper proposes a single carrier modulation technique with an optimized space vector switching sequence for multilevel inverter. Simulation results presents comparison of single and multicarrier optimized space vector switching sequence with general switching sequence of nine-level diode-clamped inverter for the parameter total harmonic distortion and fundamental component of voltage.

2. Diode-Clamped Multilevel Inverter

A three-phase nine-level diode-clamped inverter is shown in Fig.1. Each phase is constituted by 16 switches (eight switches for upper leg and eight switches for lower leg). Switches S_{a1} through S_{a8} of upper leg form complementary pair with the switches S_{a1}' to S_{a8}' lower leg of the same phase. The complementary switch pairs for phase 'A' are (S_{a1}, S_{a1}'), (S_{a2}, S_{a2}'), (S_{a3}, S_{a3}'), (S_{a4}, S_{a4}'), (S_{a5}, S_{a5}'), (S_{a6}, S_{a6}'), (S_{a7}, S_{a7}'), (S_{a8}, S_{a8}') and similarly for B and C phases. Clamping diodes carry the full load current by Jose Rodriguez et al.(2002)

Table1 shows phase to fictitious midpoint 'o' of capacitor string voltage (V_{AO}) for various switching's.

Table 1 Nine-Level Inverter Voltage States

S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}	V_{AO}
1	1	1	1	1	1	1	1	$+V_{dc}/2$
0	1	1	1	1	1	1	1	$+3V_{dc}/8$
0	0	1	1	1	1	1	1	$+V_{dc}/4$
0	0	0	1	1	1	1	1	$+V_{dc}/8$
0	0	0	0	1	1	1	1	0
0	0	0	0	0	1	1	1	$-V_{dc}/8$
0	0	0	0	0	0	1	1	$-V_{dc}/4$
0	0	0	0	0	0	0	1	$-3V_{dc}/8$
0	0	0	0	0	0	0	0	$-V_{dc}/2$

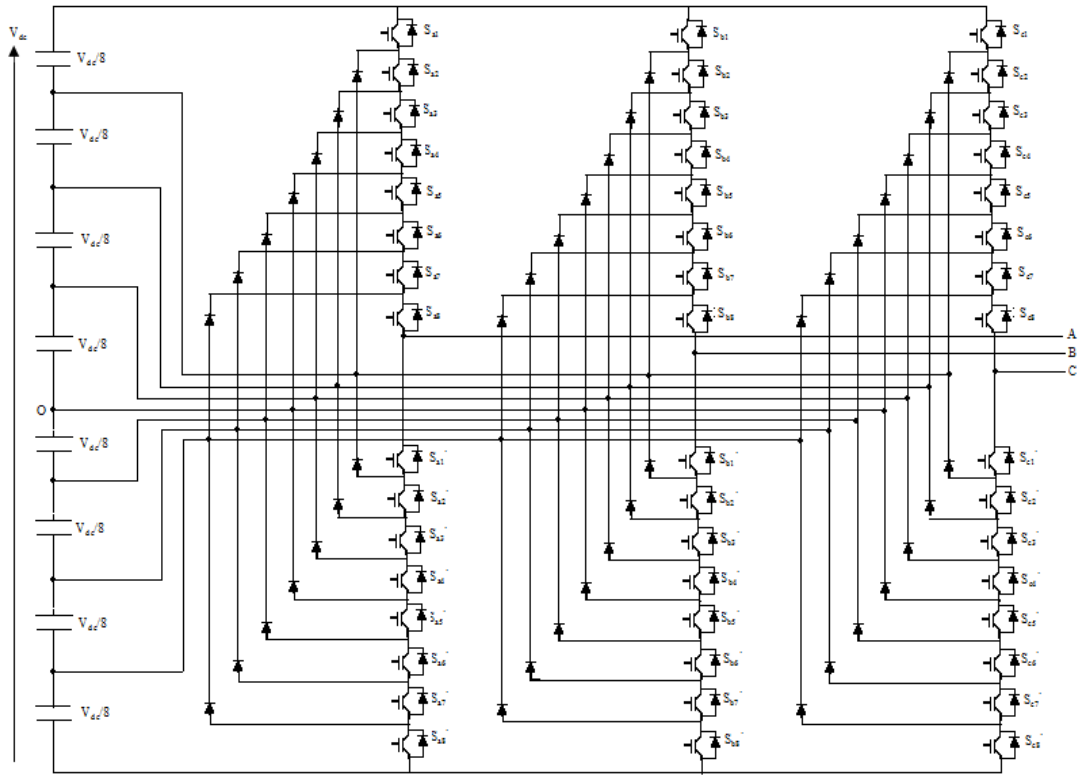

Figure 1 Circuit Diagram of 3 Phase Nine Level Diode Clamped Inverter

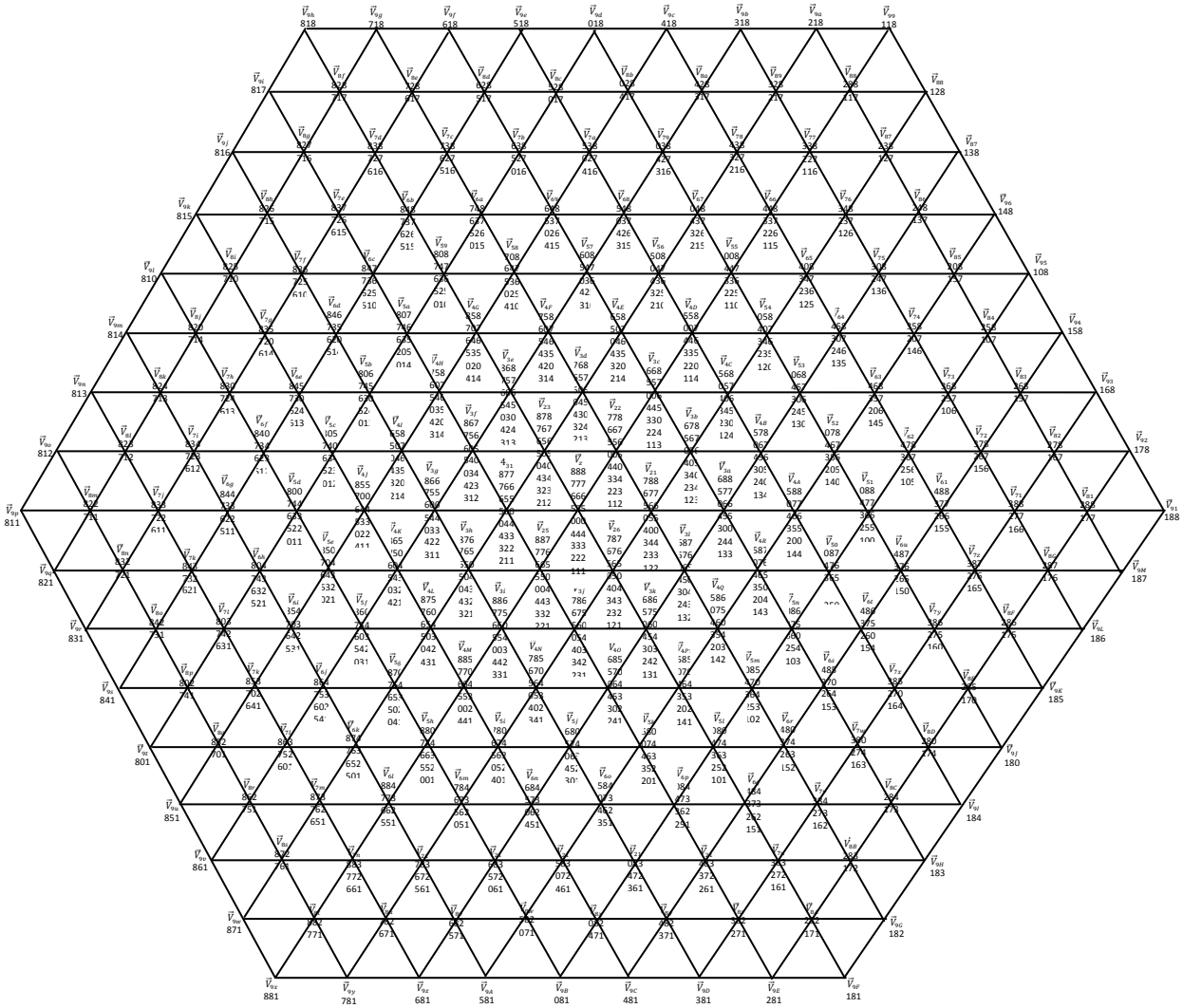

Figure 2 Nine-Level Inverter State Space Vector Diagram

3. SVPWM Implementation

Implementation of SVPWM involves (i) Identification of the sector in which the tip of the reference vector lays (ii) Determination of the nearest three voltage space vectors (ii) Determination of the duration of each of these switching voltage space vectors (iv) Choosing an optimized switching sequence.
Space vector diagram of nine-level inverter with its 729 (=3^9) vectors are shown in Fig 2. Every 60 degrees constitute a sector. Sector1 diagram is shown in Fig 3. Each sector consists of 64 regions 177 vectors.

3.1 Sector and region identification

Three phase instantaneous reference voltages (1) are transformed to two phase (2). Every 60 degrees, from zero to 360 degrees constitute a sector [4][5]. Identification of the sector in which the tip of the reference vector lies is obtained by (3).

$$V_a = V_m \sin \omega t$$

$$V_b = V_m \sin(\omega t - 2\pi/3) \qquad (1)$$

$$V_b = V_m \sin(\omega t - 4\pi/3)$$

$$V_\alpha = \frac{2}{3}\left(V_a - \frac{1}{2}(V_b + V_c)\right)$$

$$V_\beta = \frac{2}{3}\left(\frac{\sqrt{3}}{2}(V_b - V_c)\right) \quad (2)$$

$$V_{\text{ref}} = \sqrt{(V_\alpha)^2 + \left(V_\beta\right)^2} \quad ; \theta = \tan^{-1}(V_\beta / V_\alpha) \quad (3)$$

Where θ is the angle varies from 0 to 2π.

Amplitude and angle of the reference vector are obtained from (3).

From Park's transformation the di-phase, α-β components are:

$$K_1 = K_n.\left(\cos\theta - \frac{1}{\sqrt{3}}\sin\theta\right) \quad (4)$$

$$K_2 = K_n.\frac{\sin\theta}{\sin(\pi/3)} \quad (5)$$

Region is obtained by normalizing the di-phase components of the space vector (4)-(5) of an *n*-level inverter through division by V_{dc}/n-1, where V_{dc} is the dc link voltage.

3.2 Determination of the duration of nearest three voltage space vectors

Switch dwelling duration is obtained from (6)-(7).

$$T_s\vec{V}_{ref} = T_1\vec{V}_1 + T_2\vec{V}_2 + T_3\vec{V}_3 \quad (6)$$

$$T_s = T_1 + T_2 + T_3 \quad (7)$$

3.3 Determination of optimized switching sequence

Consider reference vector lying in sector1 region 21. The nearest three space vectors for switching sequence are $\vec{V}_{53}, \vec{V}_{63}, \vec{V}_{64}$.

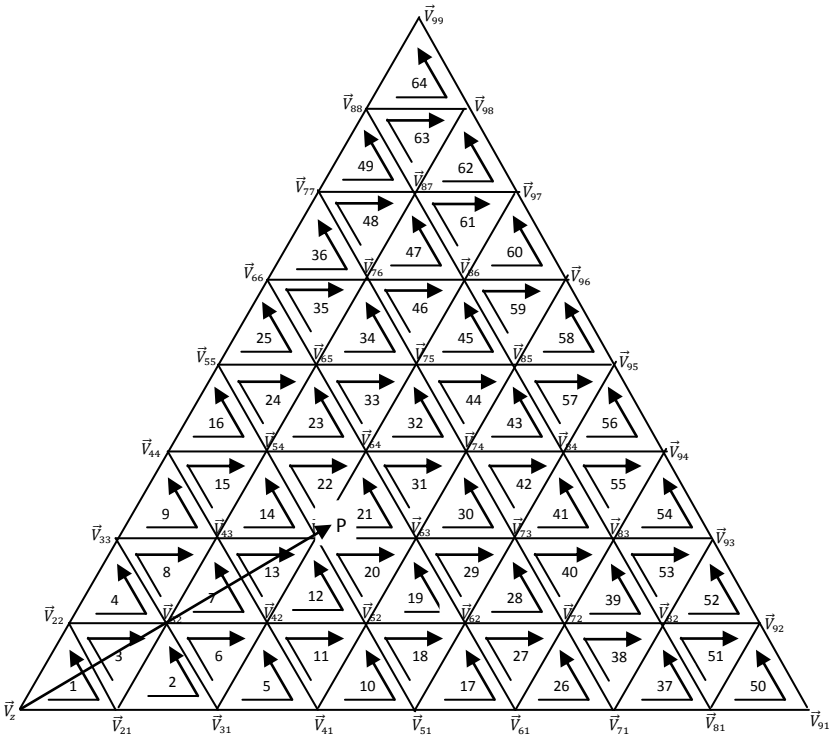

Figure 3 Sector1 Regions Space Vector Representation

The space redundant vectors for sector1 region 21, are, for $\vec{V}_{53}$ 0 6 8, 4 5 7, 3 0 6, 2 4 5, 1 3 0 (5 redundant vectors), for $\vec{V}_{63}$ 4 6 8, 3 5 7, 2 0 6, 1 4 5 (4 redundant vectors), and for $\vec{V}_{64}$ 4 5 8, 3 0 7, 2 4 6, 1 3 5 (4 redundant vectors).

An optimized switching sequence starts with virtual zero vector's state. A virtual zero vectors are with minimum offset from zero vector of two-level inverter. Based on the principles derived in literature for two-level inverter, for Region 21, switching sequence is 0 6 8→4 6 8→ 4 5 8→ 4 5 7→ 3 5 7→ 3 0 7→ 3 0 6→ 2 0 6→ 2 4 6→ 2 4 5→ 1 4 5→ 1 3 5→ 1 3 0 during a sampling interval and 1 3 0→ 1 3 5→ 1 4 5→ 2 4 5→ 2 4 6→ 2 0 6→ 3 0 6→ 3 0 7 → 3 5 7→ 4 5 7→ 4 5 8 → 4 6 8 → 0 6 8 during the subsequent sampling interval. This sequence uses all the space redundant vectors of each state by Anish Gopinath et al.(2007), (2009).

Consider two different outer regions 59 and 60 of Figure3 for switching sequence. Three vertices of region 59 are $\vec{V}_{85}$(2 0 8, 1 4 7), $\vec{V}_{86}$(2 4 8, 1 3 7) and $\vec{V}_{96}$ (1 4 8). Virtual zero vector is $\vec{V}_{85}$. The optimized switching sequence is 2 0 8 → 2 4 8 → 1 4 8 → 1 4 7 → 1 3 7 during a sampling interval and 1 3 7 → 1 4 7 → 1 4 8 → 2 4 8 → 2 0 8 during the subsequent sampling interval. Considering the region 60, Virtual zero vector is $\vec{V}_{86}$ (2 4 8, 1 3 7) and $\vec{V}_{96}$(1 4 8), $\vec{V}_{97}$(1 3 8) are the two other vertices. The optimized switching sequence is 2 4 8 → 1 4 8 → 1 3 8 → 1 3 7 during a sampling interval and 1 3 7 → 1 3 8 → 1 4 8 → 2 4 8 during the subsequent sampling interval [23]. This sequence utilizes vectors. Application of usage of same number of states also for inner regions reduced the total harmonic distortion with increased fundamental component of voltage with single carrier modulation. Extending this for region 21, the sequence is 0 6 8→4 6 8→ 4 5 8→ 4 5 7 during a sampling interval and 4 5 7→ 4 5 8 → 4 6 8 → 0 6 8 during the subsequent sampling interval discarding three redundant states from each vertex.

4. Simulation Results

Simulation is carried out on nine-level diode-clamped inverter for four methods of Space Vector PWM technique at switching frequency 1.5 KHz for different modulation indices. (i) SCMMGS-Single Carrier Multi-Modulation for General Switching Sequence (ii) MCMMGS-Multi-Carrier Multi-Modulation for General Switching Sequence (iii) SCMMOS-Single Carrier Multi-Modulation for Optimized Switching Sequence (iv) MCMMOS-Multi-Carrier Multi-Modulation for Optimized Switching Sequence.

Multi-Carrier Multi-Modulation results reduced harmonic distortion with reduced fundamental component; however Single Carrier Multi-Modulation results reduced harmonic distortion with highly improved fundamental component of voltage.

Optimized switching sequence reduces harmonic distortion compared to General switching sequence.

SVPWM-SCMMGS simulation results are shown from Figure4 through Figure7 for modulation index of 0.85. Figure4 comprises pole, phase and line voltage for SCMMGS method. Pole, phase and line voltage for MCMMGS method is Figure6. Line voltage THD for SCMMGS and MCMMGS are shown in Figure5 and Figure7 respectively.

SVPWM-SCMMOS results at modulation index of 0.85 are shown from Figure8 through Figure11. Figure8 comprises pole, phase and line voltage for SCMMOS method. Pole, phase and line voltage for MCMMOS method is Figure10. THD of line voltage is shown in Figure9 and Figure11 respectively for SCMMOS and MCMMOS.

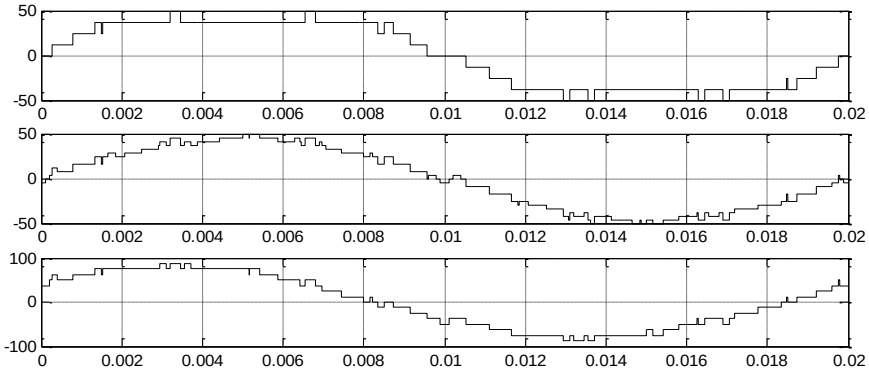

Figure 4 MCMMGS 0.85 MI Pole, Phase and Line Voltage

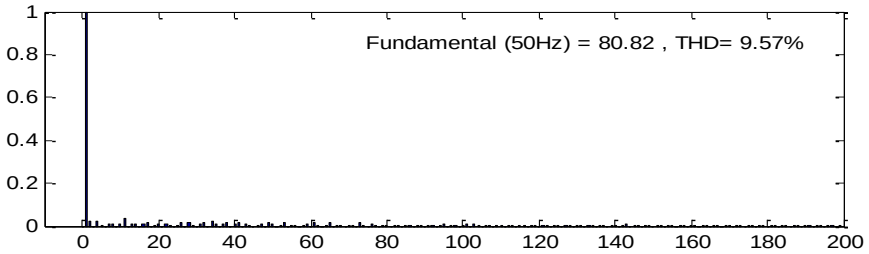

Figure 5 MCMMGS 0.85 MI Line Voltage THD

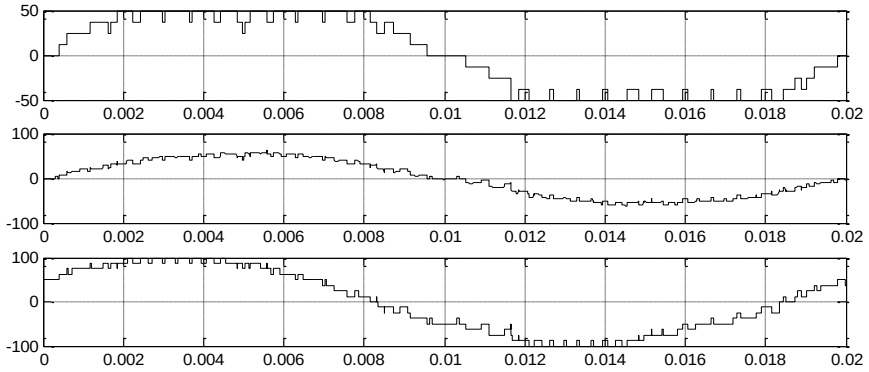

Figure 6 SCMMGS 0.85 MI Pole, Phase and Line Voltage

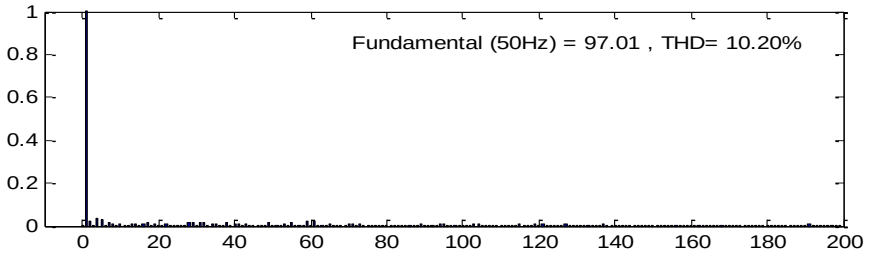

Figure 7 SCMMGS 0.85 MI Line Voltage THD

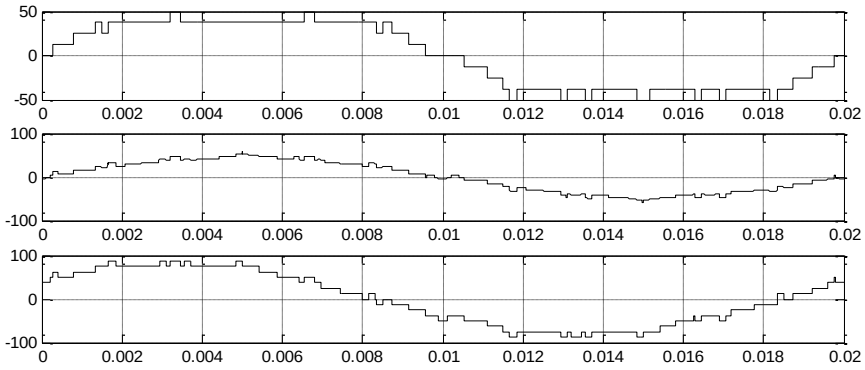

Figure 8 MCMMOS 0.85 MI Pole, Phase and Line Voltage

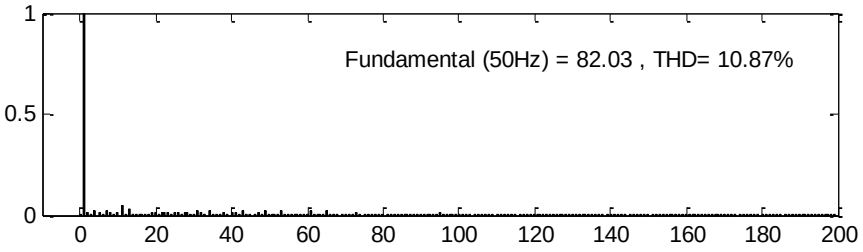

Figure 9 MCMMOS 0.85 MI Line Voltage THD

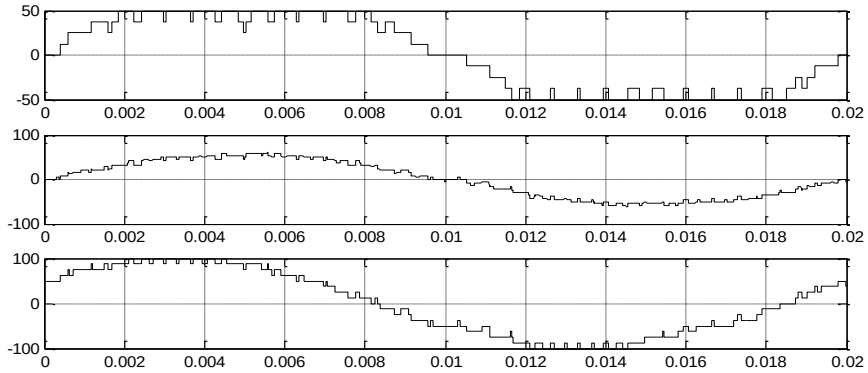

Figure 10 SCMMOS 0.85 MI Pole, Phase and Line Voltage

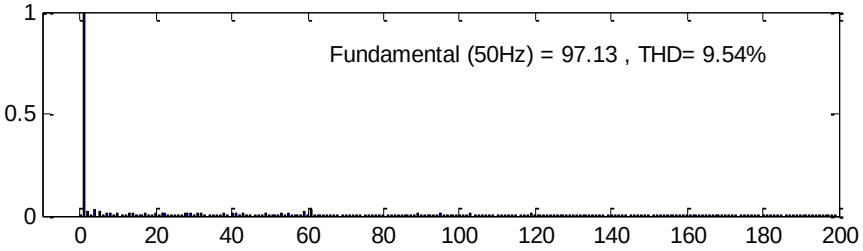

Figure 11 SCMMOS 0.85 MI Line Voltage THD

Table2 gives the Total harmonic Distortion and fundamental component of line voltage for normal modulation range.

Figure12 shows chart of Modulation Index Vs THD of line voltage.

Table 2 Modulation Index Vs THD and Fundamental Component of Voltage

MI	SCMMGS		MCMMGS		SCMMOS		MCMMOS	
	THD	V_1	THD	V_1	THD	V_1	THD	V_1
0.866	9.42	98.96	11.79	87.03	9.17	98.98	11.89	87.52
0.85	10.20	97.01	9.57	80.82	9.54	97.13	10.87	82.03
0.8	12.65	90.91	9.45	76.73	10.54	91.5	9.99	78.05
0.75	15.65	84.79	15.22	70.38	10.97	85.64	13.26	75.1
0.7	19.35	78.69	18.37	56.52	12.75	80.01	11.47	65.67
0.6	26.89	66.32	25.67	49.29	12.96	68.39	15.02	60.27

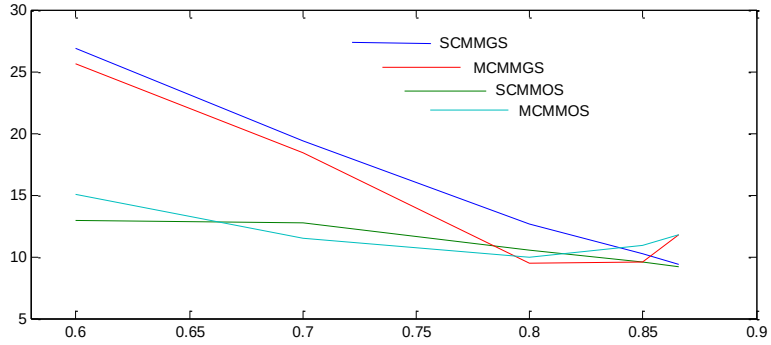

Figure 12 Mi Vs THD of Nine-Level Inverter

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