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Comparative Study of Various Systems on Chips Embedded in Mobile Devices

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ABSTRACT
Systems-on-chips (SoCs) are the latest incarnation of very large scale integration (VLSI) technology. A single integrated circuit can contain over 100 million transistors. Harnessing all this computing power requires designers to move beyond logic design into computer architecture, meet real-time deadlines, ensure low-power operation, and so on. These opportunities and challenges make SoC design an important field of research. So in the paper we will try to focus on the various aspects of SOC and the applications offered by it. Also the different parameters to be checked for functional verification like integration and complexity are described in brief. We will focus mainly on the applications of system on chip in mobile devices and then we will compare various mobile vendors in terms of different parameters like cost, memory, features, weight, and battery life, audio and video applications. A brief discussion on the upcoming technologies in SoC used in smart phones as announced by Intel, Microsoft, Texas etc. is also taken up.
Keywords: System on Chip, Core Frame Architecture, Arm Processors, Smartphone.

1. Introduction: What Is SoC?

We first need to define system-on-chip (SoC). A SoC is a complex integrated circuit that implements most or all of the functions of a complete electronic system. Exactly what components are assembled on the SoC varies with the application. Many SoCs contain analog and mixed-signal circuitry for input/output (I/O), but most of SoC's are digital because that is the only way to build such complex functions reliably. Also SoC refers to integrating all components of a computer or other electronic system into a single integrated circuit (chip). It may contain digital, analog, mixed-signals, memory, CPUs, specialized logic, busses all on a single chip substrate. A typical application is in the area of embedded systems. Many SoC products can be built using industry-standard CMOS technology for better power consumption. SoC devices incorporates most impressive ranges of cores, including 32-bit high-performance ARM- and Power based products mainly used in wireless and automotive applications.

1.1 Architecture of SoC

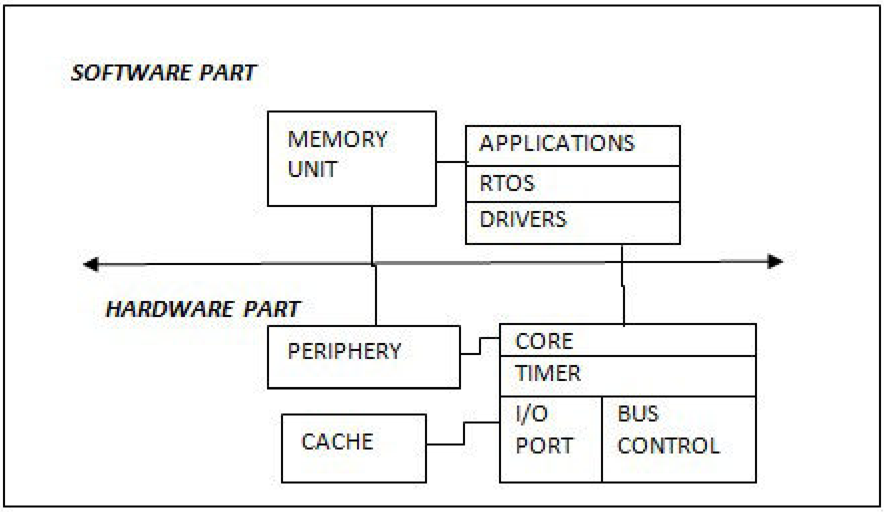

Figure 1 System on Chip Architecture

Figure 1 gives an example of typical SoC showing how the software of a programmable component can be structured on top of the hardware. Here, the real-time operating system (RTOS) includes a process scheduler. A DSP with a fixed process execution order and optimized memory communication will need fewer RTOS functions, but not so in real-time mobile applications. In other words, the heterogeneous and multifarious hardware architecture of mobile phones leads to similarly heterogeneous and multifaceted software architecture.[2]

The advantages of System on Chip include:

- Lower cost per gate.

- Lower power consumption.
- Faster circuit operation.
- More reliable implementation.
- Smaller physical size.
- Greater design security.

1.2 Comparison with Microcontroller [3]

Microcontrollers typically have fewer than 100K of RAM and are single-chip-systems; whereas the term SoC is typically used with more powerful processors, capable of running software such as Windows or Linux, which need external memory chips (flash, RAM) to be useful, and which are used with various external peripherals. In short, for larger systems System-on-a-chip is increasing chip integration to reduce manufacturing costs and to enable smaller systems.

1.3 Comparison with System in Package

When it is not feasible to construct a SoC for a particular application, an alternative is a system in package (SiP) comprising a number of chips in a single package. In large volumes, SoC is believed to be more cost effective than SiP since it increases the yield of the fabrication and because its packaging is simpler. Another option, as seen for example in higher end cell phones is ***Package on Package*** stacking during board assembly.

	System-on-chip	System-in-package
Power	Low	Medium-high
Performance (clock speed)	High	Medium
Design flexibility (features)	High	Low-medium
System design flexibility	Low	High
IP availability	Medium	High
Unit cost	Low	Medium-high
Development cost/Time	High	Low-medium
EDA tools	Mature	Limited
Available design services	High	Limited

Table 1 Comparison of SoC and SiP

On the other end is the **Complex System-on-Chip (CSoC)** that includes both digital designs and application software with particular features because of differing needs like Image processing, Spoken Language recognition, Touch sensing technologies, Multimedia Requirements etc. So various Systems on chips have been manufactured by different mobile handset manufacturers those cater various differing features offered by mobiles. [3]

While the shift towards system-on-chip processors will yield more powerful chips that are cheaper and consume less power, the chips will be less flexible. They cannot be mixed and matched with other components in the same way that today's processors can. As a result, chipmakers like Intel are trying to produce a wider range of products, each designed for a specific application or type of device. To produce such a wide range of products efficiently, future processors will have **Modular system on chips**, allowing chipmakers to quickly select the number of processor cores and other components required for a specific chip and application.

2. SOC Applications -

Systems-on-chips can be found in many product categories ranging from consumer devices to industrial systems:

- Speech Signal Processing.
- Image and Video Signal Processing.
- Information Technologies
  - PC interface (USB) Computer peripheries (printer control, LCD monitor controller, DVD controller,.etc) .
- Data Communication
  - Wire line Communication: Gigabit Ethernet, Etc
  - Wireless communication: Bluetooth, WLAN, 2G/3G/4G, WiMax etc[3]

2. 1 Issues in SoC's embedded in mobiles with proposed solutions:

2.1. A. Intel's various Processors

The system-on-a-chip (SoC) commonly adopted in handheld devices requires the close interactions among the components; hence, ***power management policy*** should be developed appropriately. So **Intel** proposed a approach that considers *dynamic voltage and frequency scaling (DVFS)* of the processor core in relation to other power consumers. The proposed policy reduces the power consumption of a mobile device by 25–42%. CPU Lincroft (Z6xx**)** is a system-on-a-chip that is aimed at smart phones and deliver up to a 50% reduction in average power consumption with full video playback and handling software including Windows 7 and Google operating systems.

Intel also launched Tolapai, a system-on-chip that includes an x86 processor, integrated chipset, and an encryption coprocessor for various appliances. Intel's Larrabee chip, under development, will pack dozens of x86 processor cores onto a single chip. It will be a programmable and highly parallel processor capable of processing graphics and visualization workloads.

Recently Intel has announced a new contract with Nokia, to deliver Atom-based system-on-chips (SoCs) having 32nm "Medfield" with CPU and NAND flash memory as the integral component to Nokia for use in their net book, smart book and Smartphone platforms. With this announcement, Intel jumps into the number one spot as Nokia's annual sales of smart phones are roughly 150M per year.

2.1. B. Samsung Hummingbird

The Hummingbird uses 45nm ARM Cortex A8 architecture at its heart with the ARMv7 instruction set, sometimes called the application processor. The 45nm manufacturing tech means that more transistors can fit on the die than in previous generations. So, the Hummingbird is estimated to gain 5-10% over ARM's original tech.

Samsung emphasizes power management while maintaining a high operating clock. Most Hummingbird cores are clocked at 1GHz, but the upcoming Infuse 4G will be clocked at 1.2GHz. Hummingbird also packs 32KB of data and instruction cache, a variable-size L2 memory cache, and the ARM NEON multimedia extension. With NEON, the Hummingbird is capable of better hardware video encoding and decoding, high quality graphics, and better sound processing.

Intrinsity changed the logic design of the standard A8 allowing certain binary operations to be run with fewer total instructions. That means the same processes are completed, but in less time

2.1. C. Qualcomm Snapdragon

The Snapdragon CPU was the first SoC that was factory clocked at 1GHz. Unlike the Hummingbird, the Snapdragon does not use an ARM-designed application processor. Rather Qualcomm designed the core (called Scorpion) to have many features similar to the ARM Cortex-A8 architecture, this meant a slight increase in instructions per clock cycle over the standard Coretex-A8.

The last generation Snapdragon chips from the Nexus One era were using the 65nm process tech. Now phones like the Desire Z, Thunderbolt, and Desire HD are using new Snapdragons on 45nm technology. Just as with the Hummingbird, this means more transistors, and better performance. Qualcomm also adds both GPS and cellular antennas to their SoC.

A chief differentiation of Qualcomm for their Snapdragon architecture is to make it a truly all-in-one solution for the various tasks on a modern Smartphone. After spending more than a decade in CDMA devices, its baseband modem chips are now integrated in the Snapdragon SoC, saving manufacturers the effort to add third party silicon.

2.1. D. Texas Instruments OMAP (Open Multimedia Application Platform)

Like Samsung, Texas Instruments licenses the Cortex-A8 from ARM, but they do not do as much modification to the core as Samsung does. Unlike other manufacturers, there are a number of models out for the OMAP SoCs. The OMAP34x series are made using the older 65nm process, the OMAP36x use the newer 45nm technology. TI has added a few interesting elements to the package to go with these cores. There is an IVA 2 imaging accelerator that supports hardware encoding of camera sensor data. This is paired with an integrated signal processor (ISP) that handles all the data crunching for image and video capture. The result is better battery performance and faster image capture.

All OMAP SoCs in the 3-series use the PowerVR SGX530 GPU. This is capable part, but is little slow compared to the GPU in the Hummingbird or new Snapdragon, but is very similar to the GPU in the iPhone 3G. OMAP also has the advantage of using the NEON ARM instruction set to boost multimedia performance. [7]

The OMAP3430 multimedia applications processor delivers up to 3x gains in performance over ARM11-based processors, enabling laptop-like productivity and advanced entertainment in mobile devices. The first application processor to be designed in a 65-nanometer (nm) CMOS process, it operates at a higher frequency than previous generation OMAP processors while lowering the core voltage and adding power reduction features.

2.1. E. Nvidia Tegra

This SoC uses dual ARM Cortex-A9 cores clocked at 1GHz. It uses the ARMv7 instruction set as well. That alone makes it notable. It will be found in devices like the Motorola Atrix phone and Xoom tablet.

The Cortex-A9 architecture uses a 40nm manufacturing process, so the transistor density is higher on this chip than the other A8-based chips. Power to the cores can be very closely monitored and controlled by the system, but both cores must be at the same power level. Tegra 2 also uses dedicated ISPs that support up to 12MP camera sensors.

Tegra may pull ahead on battery use because of the multiple caches that can keep data readily accessible to the GPU. The GeForce GPU also allows for HDMI output support

2.1. F. Nomadik

These application processors are designed specifically with mobile devices in mind, offering device manufacturers the competitive advantages in term of ultra-low power consumption for longer battery operation, unsurpassed audio, video and imaging quality, easier application development for shorter time-to-market, and scalability for multiple market segments and future multimedia applications.

2.2 Other features offered by various SoC's in Mobiles

Also one other way to reduce power consumption is to apply data encoding techniques to information transmitted on SoC buses. The buses may account up to 30 % of total power in modern processors.

The other techniques that lead to refinement of SoC architecture for low power consumption include power conscious hardware-software mapping of system's functionality. So optimisation techniques are developed considering control flow, data organisation and type of processing.[4]

Also the method of translating printed documents using hand held device is commercially available in Nokia N900 that is based on SoC OMAP 3430. Also there is feature in some smart phones to investigate the feasibility of opportunistic communications for mobile data offloading , implement a proof-of-concept prototype, called Opp-Off, which utilizes their Bluetooth interface for device/service discovery and content transfer, made possible because of functionality offered by SoC's in mobiles. [9]

2.3 RECENT DEVELOPMENTS IN FIELD OF SoC:

Beagle Board is a low-power, low-cost single-board computer produced by Texas Instruments in association with Digi-Key. The Beagle Board was designed for demonstrating the Texas Instrument's OMAP3530 system-on-a-chip. The board was developed by a small team of TI engineers as an educational board that could be used in colleges to teach open source hardware and open source software capabilities.

The Medfield platform is an Intel product with power consumption that is appropriate for smart phones employing Penwell SoC which integrates all the major components into a single chip. It is manufactured on Intel's 32nm SoC process that has been optimized for power efficiency. The process includes three transistor libraries for performance logic, standard logic and always-on blocks and extremely dense SRAM macros. [11]

Addressing the growing handset opportunity in emerging markets where consumers look for more value at lower prices, Intel also disclosed plans for the **Atom processor Z2000.** The Z2000 platform includes a 1.0GHz Atom CPU that offers enhanced graphics and video performance, and the ability to access the Web and play Google Android games. It also supports the Intel XMM 6265 3G HSPA+ modem with dual-SIM 2G/3G.

Microsoft is currently developing a version of Windows (may be **Windows 8**) that supports a variety of SoC devices, be they ARM-based (like Tegra 2, Snapdragon, OMAP) or x86-based (like Oak Trail and Fusion) that could potentially make the Windows platform all rounder.[13]

Renesas is coming up with **MP5232 SoC** which is a 1.5GHz dual-core CPU, along with HSPA+ and LTE radios on the same chip -- much like offerings from competitors Qualcomm and ST-Ericsson. [14]

Texas Instrument's CC2530 is a true system-on-chip solution tailored for IEEE 802.15.4, ZigBee, ZigBee RF4CE and Smart Energy applications. With its large flash memory of up to 256 KB, the CC2530 is ideal for ZigBee PRO applications. The larger memory sizes will allow for on-chip, over-the-air-download to support in-system reprogramming. Additionally, the CC2530 combines a fully integrated, high-performance RF transceiver with an 8051 MCU, 8 KB of RAM, 32/64/128/256 KB of Flash memory, and other powerful supporting features and peripherals.

The chip has everything you need to make a smartphone, two Cortex A9 cores (clocked at 1.5 GHz), LTE baseband, the graphics solution (supporting 1080p and 3D), the audio solution, etc. It has everything you need and production cost should be greatly reduced since the motherboard would be a lot smaller and simpler.

3. Design challenges for SoC

- Hardware and software architectures must be designed to be secure.
- Functional verification and energy efficiency to be attained.
- Providing sufficient communication performance to run the application.
- To meet the area and timing requirements
- Software developed must be high performance, real time, and low power consuming.[5]

In any processor-driven design, a number of peripheral devices are needed. These include timers, DMA Controllers, interrupt controllers, and memory controllers. In many cost-sensitive applications, a shared memory structure is utilized to reduce memory component costs. So architecture is needed that addresses the memory needs of all devices without severely degrading the performance of any single device.

Most existing buses were designed to connect discrete devices on a PCB substrate. At the board level, a key issue is minimizing the number of bus signals because pin and signal count translates directly into package and PCB costs. A large number of device pins reduces component density on the board. This is why traditional system level buses use shared tri-state signalling and, multiplexed address and data on the same signals.

But synthesis tools find it difficult to deal with shared tri-state signals with several drivers and receivers connected to the same trace. Static timing analysis is difficult and often the only way to verify timing is to use a circuit level simulator such as Spice. All of this takes time and effort without adding real value in terms of device functionality or features. Bus loading also limits theoretical performance.

With more new phones offering digital cameras, MP3 players, handheld game devices research scientists will have to find how best to connect all of those non-phone peripherals with an application coprocessor in handsets. So the solution offered is Core Frame Architecture.

3.1. A. Test parameters to verify performance

A System on Chip (SoC) is an implementation technology, not a market segment or application domain. SoC's may have many shapes and many different variants, so the verification of an SoC is carried out by stimulating it, checking that it adheres to the specification and exercise it through a wide set of scenarios.

So performance of SoCs is to be checked on the basis of following parameters:

Integration: The primary focus in SoC verification is on checking the integration between various components. The underlying assumption is that each component was already checked by itself.

Complexity: The combined complexity of the multiple sub-systems can be huge, and there are many seemingly independent activities that need to be closely correlated. As a result, we need a way to define complicated test scenarios.

Reuse of IP blocks: The reuse of many hardware IP blocks in a mix-and-match style suggests reuse of the verification components as well. Many companies treat their verification IP as a valuable asset (sometimes valued even more than the hardware IP).

HW / SW co verification: The software or firmware running on the processor can be verified only in relation to the hardware. But even more than that, we should consider the software and hardware together as the full Device under Test (DUT), and check for scenarios that involve the combined state of both hardware and software.[10]

3.1. B. Solution: Core Frame Architecture

PALMCHIP developed a system-on-chip bus architecture called Core Frame to meet the unique requirements of SOC based designs. The Core Frame architecture differs significantly from other on-chip buses. By using point-to-point signals instead of shared tri-stated lines, it delivers higher performance while simultaneously reducing design and verification effort.

The Core Frame architecture was developed with several concerns in mind:

- It must be processor and technology independent
- It must be easily synthesizable and flexible
- It must be cantered around shared memory
- It must not sacrifice performance
- It must not add cost to a design

To address these concerns, the Core Frame architecture includes:

- 400 MB/s bandwidth at 100 MHz
- Support for 32-, 16- and 8-bit peripherals
- Unidirectional busses only
- Positive-edge clocking only
- A central, shared memory controller
- Single clock cycle data transfers
- Separate peripheral I/O and DMA busses
- Application-specific memory map and peripherals

The most distinctive feature of Core Frame is the separation of I/O and memory transfers onto different buses. The architecture centres on the Palm Bus and the MBus. The Palm Bus is designed for low-speed accesses from the CPU core. The MBus is designed for high-speed accesses to external memory from the CPU core or peripheral blocks.

Energy-Aware System Design: Algorithms and Architectures provides state-of-the-art ideas for low power design methods from circuit, architecture to software level and offers design case studies in three fast growing areas of mobile storage, biomedical and security.[1]

4. RESULT: Comparison of Various Soc's In Mobiles

There are several advances in chip miniaturization and raw speeds that are happening lately. Smartphone pose the most difficult task – to combine performance with the lowest power consumption possible, and thus play a huge role in the mobile processing war.

The world of mobile SoCs is a wild one. Each company has its own philosophy when it comes to designing a chip.

Some, like TI and Samsung, like to stick to the ARM architecture and design packages around it. But Qualcomm has designed a custom monster of a SoC, and their integrated designs have been a boon for manufacturers. A good example of this is Nvidia's Tegra 2.

Qualcomm, Samsung, Apple and Texas Instruments are currently the major SoC players, and they have something in common – all of their chipsets are based on the ARM architecture. ARM Holdings owns the intellectual property rights on processor architecture; they develop the next generation's schematics, and then sell them to chip manufacturers to come up with their own custom SoC solutions. The current 1GHz mobile CPUs are based on ARM's Cortex-A8 generation, but Cortex-A9 is just around the corner, and it is exciting.

The prevailing concern for the company was to make a mobile SoC that can go all day on a single charge, thus Snapdragon was designed with low power consumption in mind. For the graphics tasks, Qualcomm relies on the AMD Z430 processor after purchasing Imageon - the mobile graphics department of AMD, and then rebadged their GPUs under the Adreno moniker.

4.1 So here is presented a brief comparison of various functionalities and the features offered by the System on Chip of various mobile phones

Serial No.	System on Chip	Mobile Phones using SoC	Processor used	Special Features	Manufacturer
1	Canmore, Sodaville, Moorsetown	Apple i-phone	600 MHz ARM Cortex-A8	Cater power sensitive needs	Intel
2	Orion	Samsung	1GHz ARM Cortex-A9 cores	Enhanced 3D graphics performance and onboard display controller.	Samsung (Competition for Qualcomm)
3	Snapdragon's Scorpion	HD2, Nexus One, and Evo 4G, Desire Z, Thunderbolt	Application co-processor similar to ARM Cortex-A8 core and based on the ARM v7 instruction set	Real-time computing with low power consumption for day-long battery life, higher performance for multimedia-related operations and GPS.	Qualcomm
4	Open Multimedia Application Platform (OMAP)	Nokia's N-series range, Palm Pre, Open Pandora, Motorola Droid, Sony Ericsson Satio and Vivaz, and the Samsung OMNIA HD.	Cortex-A8 from ARM	Delivers High Performance, Basic Multimedia and Modem Applications	Texas Instruments
5	OMAP4	BlackBerry Playbook.		PowerVR SGX540 GPU provides a faster IVA 3 image accelerator	Texas Instruments
6	Nomadik	ST- Ericsson	ARM architecture.	multimedia applications and 2.5G/3G mobile phones	Semiconductor Technology
7	Tegra	Samsung M1, LG Optimus, Motorola Atrix phone	dual-core ARM Cortex-A9	emphasizes low power consumption and high performance	NVIDIA
8	Nexperia Cellular		ARM architecture.	JPEG, MPEG-4, MP3, A/V streaming and GPS, cost-effective GPRS	Philips
9	Intel's Xscale			single-chip camera	TransChip
10	Athlon			Integrated the memory controller with the processor on a single chip.	Advanced Micro Devices Inc
11	Hummingbird	Galaxy S Android phone	ARM NEON	power management , high operating clock ,better hardware video and sound processing	Samsung
12	The A4	Apple i-phone			Intrinsity

Table 2. Comparison of Various Soc's In Mobiles

Thus it is seen the markets of mobiles SoC's moving towards more competitive applications in terms of software and hardware. And we compared the features offered by various processors in the mobiles. The main added value of Samsung's Hummingbird chipset, compared with the other current hardware platforms is in the graphics subsystem. It is built around a PowerVR SGX 540 core, with theoretical processing of up to 90mln triangles per second. The 2D performance of the Hummingbird is better with an even larger margin – a billion pixels per

second versus half a billion for the dual-core Snapdragon and the end result are outstanding, and on par with what mobile gaming systems are achieving.
The 3GS successor, the iPhone 4, is having a custom designed chipset called A4, which is running the iPad as well. Samsung developed the Hummingbird platform based on intellectual property from Intrinsity, a processing solutions company.

4.2 Now the comparison of various mobile phone vendors in terms of sales is presented in following table.

Source	Date	Nokia	SAMSUNG	LG	Apple	RIM	Sony Ericsson	Others
IDC	Q1/2010	36.6%	21.8%	9.2%	---	3.6%	3.6%	25.3%
Gartner	Q1/2010	35.0%	20.6%	8.6%	---	3.4%	3.1%	29.3%
Gartner	Q3/2010	33.8%	21.8%	8.7%	4.3%	3.8%	---	27.6%

Table 3. Comparison of Various Mobiles in terms of sales

We observed that the mobile Phones having TI OMAP as processors has high shipment rate. The 5th generation OMAP, OMAP 5 SoC uses a dual-core ARM Cortex-A15 CPU with two additional Cortex-M4 cores to offload the A15s in less computationally intensive tasks to increase power efficiency, two PowerVR SGX544MP graphics cores and a dedicated TI 2D Bit graphics accelerator, a multi-pipe display sub-system and a signal processor. They respectively support 24 and 20 mega pixel cameras for front and rear 3D HD video recording. The chip also supports up to 8 GB of dual channel DDR3 memory, output to four HD 3D displays and 3D HDMI 1.4 video output. OMAP 5 also includes 3 USB 2.0 ports and a SATA 2.0 control.
Samsung has first launched the Exynos 4210 SoC within its Samsung Galaxy S II mobile Smartphone. The driver code for the Exynos 4210 was made available in the Linux kernel.
And later Samsung introduced Exynos 4212, as a successor to the 4210 that features a higher clock frequency and 50 percent higher 3D graphics performance over the previous processor generation. Built with 32 nm High-K Metal Gate (HKMG) low-power process it promises 30 percent lower power-level over the previous process generation.

5. Conclusion

This survey paper digs into the details of various SoC used in mobiles with focus on the functionality and applications offered that is largely dependent upon the processor chip capabilities. After study it is concluded that the issues of power consumption and space savings on the mobile chip can be resolved by using Core frame Architecture instead of tri signal sharing of buses. This also brings in more reliability, higher design security and faster circuit operation.
As Intel, Samsung and Texas Instruments are found to be the major players in the field of SoC research and they have come up with the power processors such as Lincroft, Hummingbird and OMAP 4430 SoC's, mostly incorporating ARM cortex A-8 processor based on 60 nm technologies as a centralised brain of the device. Recently developed Medfield, CC2530 SoC's will be using ARM Cortex A-9 based on 32 nm technique and ZigBee RF4CE respectively to provide for superb power efficiencies and other powerful supporting features and peripherals.
Area where Hummingbird SoC has upper hand is Screens display Quality, Screen size which is good enough for games and watching movies, faster Web browsing, Camera's features like touch focus and pinch to zoom, video (1080p@30fps) quality and the image quality (8 MP, 3264×2448 pixels, auto focus, LED flash) etc. possible because of dual-core ARM Cortex A9 1.2 GHz processor and 1 GB of RAM.But Texas Instruments has announced a Cortex-A9 chipset that will be available for Smartphone, that will provide multiple core operation, dual-channel memory controller, efficient instruction handling up to the application level, and overall superior power management, superior image processing and stabilization technologies .
So it can now be said that as the new processors are coming into the market, more and more advanced up gradations are expected and thus the competition is rising in terms of clock speed and energy efficiency.

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