Innovative Systems Design and Engineering
ISSN 2222-1727 (Paper) ISSN 2222-2871 (Online)
Vol 3, No 5, 2012

Array Multiplier using pMOS based 3T XOR Cell

Shiwani Singh[1] Tripti Sharma[2*] K. G. Sharma[2] Prof. B. P. Singh[1]

1. Electronics and Communication Engineering Department FET-MITS(Deemed University) Lakshmangarh, Distt.-Sikar, India

2. Electronics and Communication Engineering Department Suresh Gyan Vihar University, Jagatpura Jaipur, Rajasthan, India

* E-mail of the corresponding author: tripsha@gmail.com

Abstract

This paper proposes a 3T XOR gate design consisting of pMOS transistors. This new design of XOR cell has been compared with existing 3T XOR design and significant improvement in PDP (Power-Delay Product) has been obtained. As an application of proposed XOR gate, a 2×2 array multiplier has been designed which also shows promising performance than existing one. All simulations are performed on 45nm standard model on Tanner EDA tool version 13.0.

Keywords: 3T (3 transistor), XOR gate, 2×2 array multiplier and PDP (Power-Delay Product).

1. Introduction

Low-power design of VLSI circuits has been identified as a critical technological need in recent years due to the high demand for portable consumer electronics products. The multiplier is one of the important functional blocks of an ALU. An array multiplier is a simplest one among all other multipliers because of its regular structure and the XOR gate is the most power consuming and essential component of an array multiplier, therefore, to enhance the overall performance of multiplier, it is must to improve the XOR gate performance. The design of XOR has been undergoing a considerable improvement, being motivated by the basic design goals, viz. minimizing the transistor count, minimizing the power consumption and high throughput (N. Weste, *et. al, 2011*; S. Kang, *et. al,* 2003).

This paper proposed a pMOS based 3T XOR cell. The pMOS has an advantage of reducing power consumption with increasing temperature with the scaling down of technologies. This happens due to NBTI effect which demonstrates the negative shift of threshold voltage caused by variation in temperature. Also the Fermi potential of the pMOS reduces with increase in temperature and as a result the device threshold voltage will also decrease. Since power consumption is proportional to threshold voltage, so it will also reduce.

As an application of the proposed 3T XOR gate, a 2×2 array multiplier has been designed and its performance has been analyzed and compared in terms of PDP with varying input voltage and temperature and noise immunity with its peer design using existing 3T XOR gate.

The paper is organized as follows: The basics of array multiplication are included in Section 2, Section 3 introduces the proposed 3T XOR cell and Section 4 illustrates 2×2 array multiplier design. Simulation results and their comparisons are included in Section 5 and finally Section 6 concluded the paper.

2. Basics of Array Multiplier

The most basic form of multiplication consists of forming the product of two unsigned number. M×N-bit multiplication can be viewed as forming N partial products of M bits each and then summing the appropriately shifted partial products to produce an M+N-bit result P. An array multiplier is easy to design because of its regular structure and may be pipelined to decrease clock period at the expense of latency. The limitation of an array multiplier is the increase in size with increasing operands. Array multiplier has a regular structure that simplifies the wiring and the layout. The basic process of binary array multiplication involves the AND operation of multiplicand

and multiplier bits and subsequent addition. An N×N array multiplier requires; N (N-2) full adders, N half adders and N^2 AND gates. Fig.1 shows the block diagram of 2x2 array multiplier consisting of 04 AND gates and 02 half adders as calculated from the given formula (J.P. Uyemura 2002; N. Weste, *et. al,* 2011).

The 2×2 array multiplier consists of:

- Four 2-input AND gates: The AND gate used in design of array multiplier is implemented using conventional CMOS technology in order to provide full voltage swing at the first stage of multiplier design. The schematic of AND gate [1] - [3] is shown below in Fig. 2
- Two half adders: The Sum module of half adders used in the circuit is implemented by existing and proposed 3T XOR gate while the Carry Module has been designed using conventional CMOS AND gate consisting of six transistors.

  The existing XOR gate used in the design of array multiplier is implemented using a modified version of a CMOS inverter and a pMOS pass transistor as shown in Fig. 3. ()

The existing 3T XOR cell designed by Tripti Sharma, *et. al,* (2010); D.Wang, *et. al,* (2009); S. Veeramachaneni, *et. al,* (2008) and S. R. Chowdhury, *et. al,* (2008) and proposed 3T XOR cells have been used to implement 2×2 array multiplier to significantly reduce the power consumption and the chip area of array multipliers, without sacrificing performance. The approach behind this is to use low power, minimal transistor count XOR gates that are the most power consuming blocks in the design of multiplier.

3. Proposed pMOS 3T XOR cell

The schematic of proposed 3T XOR cell is shown in Fig.4. It consists of 3 pMOS transistors and a negative input supply voltage of 250 mV is given to M3 so that it eliminates the negative voltage spikes for input combination '00'. The W/L ratios of transistors M1and M2 are taken as 3/1 to minimize the affect of M3 and to take output node at logic high.

Case1: When AB=00, all transistors are ON and as pMOS is weak '0' device, it will pass low logic signal with threshold loss. But at the same time due to parallel resistances of ON transistors there will be slight reduction in threshold loss and nearly 4% degradation in the output is obtained.

Case 2: When AB=01 and AB =10, M1 & M2 are ON respectively and pMOS being strong '1' device will allow to pass complete logic high at the output. But as M3 is always and connected to ground, hence it will try to pull the output node towards ground. Therefore to overcome the affect of M3 and to charge the output node at logic high, aspect ratios of M1 and M2 are increased to 3/1 with respect to M3 i.e.; 1/1.

Case 3: For AB=11, only M3 is ON and it will pass low logic signal with threshold loss.

The performance table shown in Table 1 illustrates the small degradation in the output voltage with respect to the full scale input voltage value which can be easily interpreted as logic '1'. However, the proposed design for XOR gate gives better performance than existing one.

For a pMOS transistor, Fermi potential is given by Equation (1) as given below

$$\varphi_F = -K_bT/q \quad \ln (N_{sub}/n_i) \qquad (1)$$

Where, N_{sub} is the substrate doping concentration and n_i is the intrinsic carrier concentration.

The gradient of φ_F with respect to the temperature is given by Equation (2) as given below

$$d\varphi_F/dT = 1/T\,[\varphi_{F+} 3K_bT/2q \quad + E_{g0}/2q] \qquad (2)$$

The parameter φ_F always decreases in absolute value when the temperature increases. For a pMOS transistor, φF is negative and dφF/dT is positive while for nMOS, φ_F is positive and $d\varphi_F/dT$ is negative.

By assuming that the oxide charge is temperature independent, the Fermi potential dependence of threshold voltage, V_{th0} is given by Equation (3) given below (Michael S-C Lu1, *et. al,* 2006)

$$V_{th0} = \varphi_{GB} - Q_{ox}/C_{ox} + 2\,\varphi_{F+}\, Q_d/C_{ox} \qquad (3)$$

Where, φ_{GB} is work function difference between channel and gate, Q_{ox} is charge density Q_D *is* depletion region charge density. Since, φF is negative for pMOS and is positive for nMOS, thus, it can be concluded from Equation (2) and Equation (3) that with increasing temperature, decrement in φ_F leads to decrement in threshold voltage of pMOS transistor and increment in threshold voltage of nMOS transistor. Thus, a gradual shift of threshold voltage over time is observed in pMOS transistor. This shift is caused by voltage stress on the gate oxide, temperature, and the duty cycle of the stressing voltage. This effect becomes more severe with reduced transistor dimensions and lower operating voltages. Austin Lesea, *et. al,* (2005) discovered this phenomenon of negative shift of threshold voltage is called pMOS Negative Bias Temperature Instability (NBTI) From Einstein's relation given below in Equation (4), it is clear that on increasing temperature, mobility decreases. (Streetman, *et. al,* 2001)

$$D/\mu = kT/q \quad (4)$$

And as mobility decreases, from Equation (5) it is obvious that decreasing mobility will increase delay. (S. Kang, *et. al,* 2003)

$$t_p = C_{load} \ / \ \mu(W/L)\ (V_{DD}-V_t)\ [2V_t/(V_{DD}-V_t) + \ln\ (4(V_{DD}-V_t)/V_{DD}\ -1)] \quad (5)$$

The better metric to evaluate a circuit's performance is PDP which removes the conflict between power consumption and delay.

Table 2 and 3 illustrates the PDP of both the designs with increasing voltage and temperature. The PDP of the proposed cell decreases with increment in temperature in accordance with above Equation. (1) – (5) and as the temperature increases the difference between the PDP of proposed XOR cell and existing cell is increasing thereby showing 2%-43% improvement of proposed cell over existing one.

4. 2×2 Array Multiplier Design

The schematic of 2×2 Array multiplier using existing and proposed XOR cell is shown in Fig.5 and Fig. 6 respectively. The array multiplier designed using existing XOR gate gives threshold loss for some input combinations and thus the output may mistakenly interpreted as logic low which is not desirable for high performance systems.

On the other hand, the proposed design operates efficiently in super threshold region to achieve low power. This circuit improves threshold loss up to 20% when compared with existing design. Although, it shows small voltage drop for certain input combinations but this drop is so less that it can be assumed as logic high. It also improves PDP and output noise voltage which is of great interest in the complex circuit design. Hence this proposed design acts as better alternative to be used in power efficient complex systems with optimum performance.

5. Simulation and Comparison

All the simulations of the proposed and the existing designs have been performed using Tanner EDA Tool version 13.0 on 45nm process technology for low-power applications with increasing input voltages from 0.5V to 1V in steps of 0.1V.

In order to prove that proposed design is consuming low power and has high performance; simulations are carried out for PDP at increasing input voltage and temperature. Simulations are also done for extracting noise immunity of existing and proposed designs. The complete input stream covering all possible combinations has been used to prove the proper functioning of the circuits.

The graphs shown in Fig. 7 – Fig. 9 depicts that the multiplier design using proposed 3T XOR cell is a viable option for power efficient design as it is maintaining the high performance of its main building block i.e.; XOR cell.

Fig. 7 reveals that the PDP of proposed design is reduced than the existing one. Even at varying temperature, PDP of the proposed design is improved in comparison to existing one as shown in Fig. 8. Fig. 9 reveals less output noise voltage of the proposed design ensuring the better noise immunity of proposed cell.

6. Conclusion

The 2×2 array multiplier has been designed using a new 3T XOR cell implemented by pMOS transistors only. The PDP of multiplier implemented using proposed XOR cell is remarkably improved with respect to increasing input voltage as well as increasing temperature when compared to existing design. Hence in a nutshell the proposed array multiplier proves itself to be a better option for low power devices and systems than its peer design.

References

N. Weste and K. Eshraghian (2011), "CMOS VLSI Design, A Circuits and Systems Perspective", (4th ed.). Addison- Wesley, (Chapter- 9 and Chapter-11)

S. Kang and Y. Leblebici, (2003), "CMOS Digital Integrated Circuits, Analysis and Design", (3rd ed.). Tata McGraw-Hill, (Chapter-6)

J.P. Uyemura, (2002), "Introduction to VLSI Circuits and System", (3rd ed.). John Wiley and Sons, (Chapter-13)

S. R. Chowdhury, A. Banerjee, A. Roy, H. Saha (2008), "A high speed 8-transistor full adder design using novel 3 transistor XOR gates", *International Journal of Electronics, Circuits and Systems*, vol. 2, No. 4, 217-223.

S.Veeramachaneni, , M.B.Srinivas (2008), "New Improved 1-Bit Full Adder Cells", *CCECE/ CCGEI*, Niagara Falls. Canada, 735-738.

D.Wang, M.Yang, W.Cheng, X.Guan, Z.Zhu, Y.Yang (2009), "Novel Low Power Full Adder Cells in 180nm CMOS Technology", *Prod. IEEE ICIEA* pp. 430-433.

Tripti Sharma K.G.Sharma, Prof.B.P.Singh, Neha Arora (2010), A Novel CMOS 1-bit 8T Full Adder Cell *World Scientific and Engineering Academy and Society (WSEAS) Transactions on Systems*, Vol. 9, No.3, 317-326

Austin Lesea, Andrew Percey (2005), "Negative-Bias Temperature Instability (NBTI) Effects in 90 nm PMOS", , *XilinxWP224 (v1.1)*, 1-4.

Michael S-C Lu1, Dong-Hang Liu, Li-Sheng Zheng Sheng-Hsiang Tseng (2006), "Micromachined structures using transistors in the subthreshold region for thermal sensing" , *Journal of micromechanics and microengineering*, 1734-1739.

Ben G. Streetman S. Banerjee, (2001), "Solid State Electronic Devices", (5th ed.). Prentice-Hall of India, (Chapter-4)

Ms. Shiwani Singh was born in Bareilly, Uttar Pradesh, INDIA on 28/08/1988. She has done B.Tech in Electronics and Communication Engineering from the Faculty of Engineering & Technology, Mody Institute of Technology and Science, Rajasthan, INDIA in 2010. Presently, she is pursuing M.Tech. in VLSI Design from same university.

Mrs. Tripti Sharma was born in Allahabad, Uttar Pradesh, INDIA on 18/10/1979. She earned B.E. degree in Electronics Engineering from North Maharashtra University in 2001 and M Tech. degree in VLSI Design from Faculty of Engineering & Technology, Mody Institute of Technology and Science, Rajasthan in 2010. Presently, she is pursuing Ph.D. in the field of low power high performance digital VLSI circuit design from Suresh Gyan Vihar University, Jaipur.

After stepping into professional world, she started as lecturer with C.S.J.M University, Kanpur and continued it up to late 2003. After that she joined Faculty of Engineering & Technology, Mody Institute of Technology and Science, Rajasthan. Her working habits and discipline made her popular among the university and she was later awarded with designation of Asst. Professor in 2009. Her current research interests include digital VLSI circuits. She has over 30 papers published in International and national Journals and more than 10 presentations in International and National Seminars / Symposia/ Conferences. Mrs. Sharma is the life member of Indian Society of Technical Education

(ISTE).

Mr. K. G. Sharma was born in a village Rura, Kanpur, Uttar Pradesh, INDIA. K.G. Sharma received the B.E. degree in Electronics and Communication Engineering from Madan Mohan Malviya Engineering College, DDU University, Gorakhpur in 2001 and completed his M Tech. degree in VLSI design from Faculty of Engineering & Technology, Mody Institute of Technology and Science in 2009. Now he is pursuing his Ph.D. degree in the field of low power VLSI circuits from from Suresh Gyan Vihar University, Jaipur.

He demonstrated his skills in Research & Development of Industrial Electronics, Kanpur for a briefer period and then he shifted to Academics and shared his knowledge as lecturer at renowned university in Kanpur in the initial stages of his career. He extended his profession as faculty of Engineering and Technology in MITS from 2003 and with experience promoted to Asst. Professor in the same university. Because of his extensive research work, he has more than 40 research papers published in various international/ national journals and conferences. Mr. Sharma is the life member of Indian Society of Technical Education (ISTE).

Prof. B. P. Singh was born in a village Orro, Nawadah, Bihar, INDIA in 1947. He did B.Sc. (Engg.) and M.Sc. (Engg.) from Bihar Institute of Technology, Sindri, Dhanbad and B.I.T. Mesra Ranchi in 1967 and 1970. He did Ph.D. from Ranchi University Ranchi in 1980. He served B.I.T. Mesra, Ranchi from 1970 to 1981, Indian School of Mines Dhanbad from 1981 to 1987 and Madan Mohan Malaviya Engg. College from 1987 to 2009. From 2009 till date he is the H.O.D. of ECE and EEE, Mody Instiute of Technology Lakshmangarh, Sikar, Rajasthan (INDIA). He has over 50 papers to his credits in International and national Journals and over 50 presentations in International and National Seminars / Symposia/ Conferences. His area of research is device modeling, low-power and high performance integrated circuit design and emerging CMOS technologies. Prof. Singh is the senior fellow of IEEE and life member of IETE.

Table 1. Performance Table of Existing and Proposed 3T XOR cell

A (Volt)	**B (Volt)**	**Expected Output (Volt)**	**Obtained Output (Volt)**	
			Existing 3T XOR Cell (Fig. 3)	**Proposed3T XOR Cell (Fig. 4)**
0	0	0	-0.13	0.047
0	1	1	0.99	0.84
1	0	1	0.76	0.84
1	1	0	0	0.073

Table 2. PDP of Existing and Proposed 3T XOR cell with increasing input voltage

Input Voltage (volt)	PDP (watt-sec)	
	Existing 3T XOR Cell (Fig. 3)	Proposed 3T XOR Cell (Fig. 4)
0.5	4.0650e-0014	3.8095e-0014
0.6	8.3707e-0014	5.7479e-0014
0.7	1.5939e-0013	7.9953e-0014
0.8	2.2107e-0013	1.0529e-0013
0.9	2.9716e-0013	1.3462e-0013
1	3.8353e-0013	1.6616e-0013

Table 3. PDP of Existing and Proposed 3T XOR cell with increasing temperature

Temperature (ºC)	PDP (watt-sec)	
	Existing 3T XOR Cell (Fig. 3)	Proposed 3T XOR Cell (Fig. 4)
-10	2.2538e-0013	1.1090e-0013
0	2.2625e-0013	1.0916e-0013
20	2.2217e-0013	1.0600e-0013
40	2.1788e-0013	1.0330e-0013
50	2.1588e-0013	1.0209e-0013
60	2.1394e-0013	1.0091e-0013

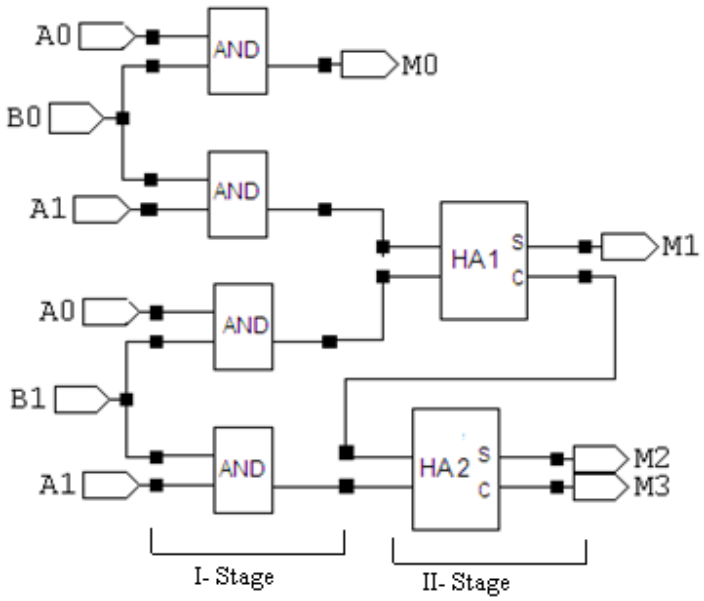

Figure 1. Block Diagram of 2x2 Array Multiplier

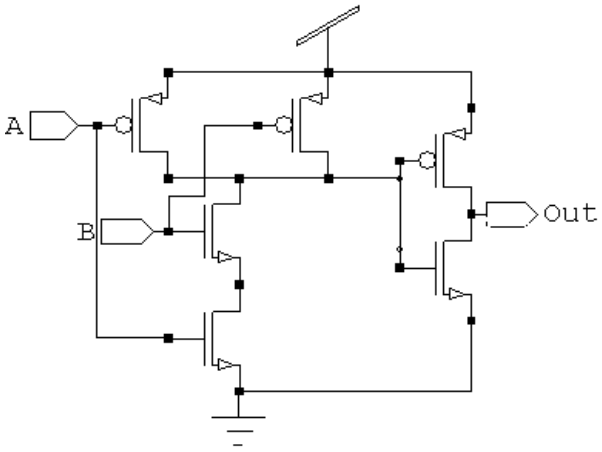

Figure 2. CMOS AND gate

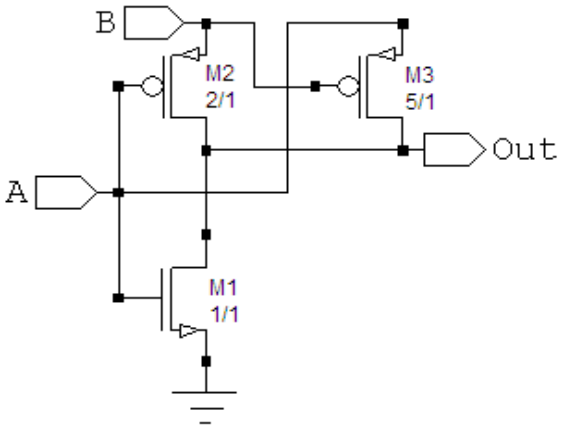

Figure 3. Schematic of existing 3T XOR cell

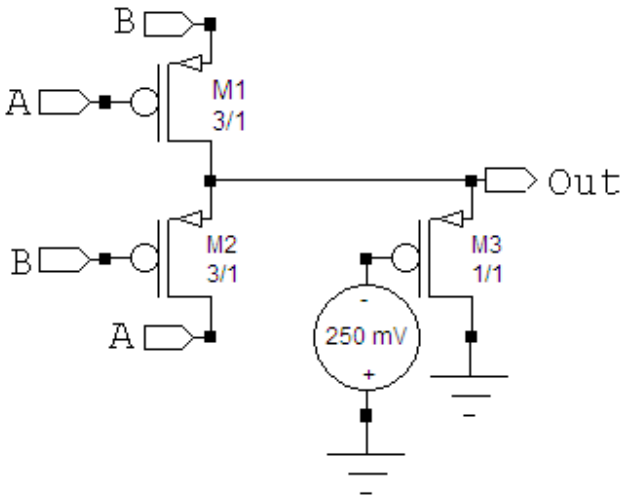

Figure 4. Schematic of proposed 3T XOR cell

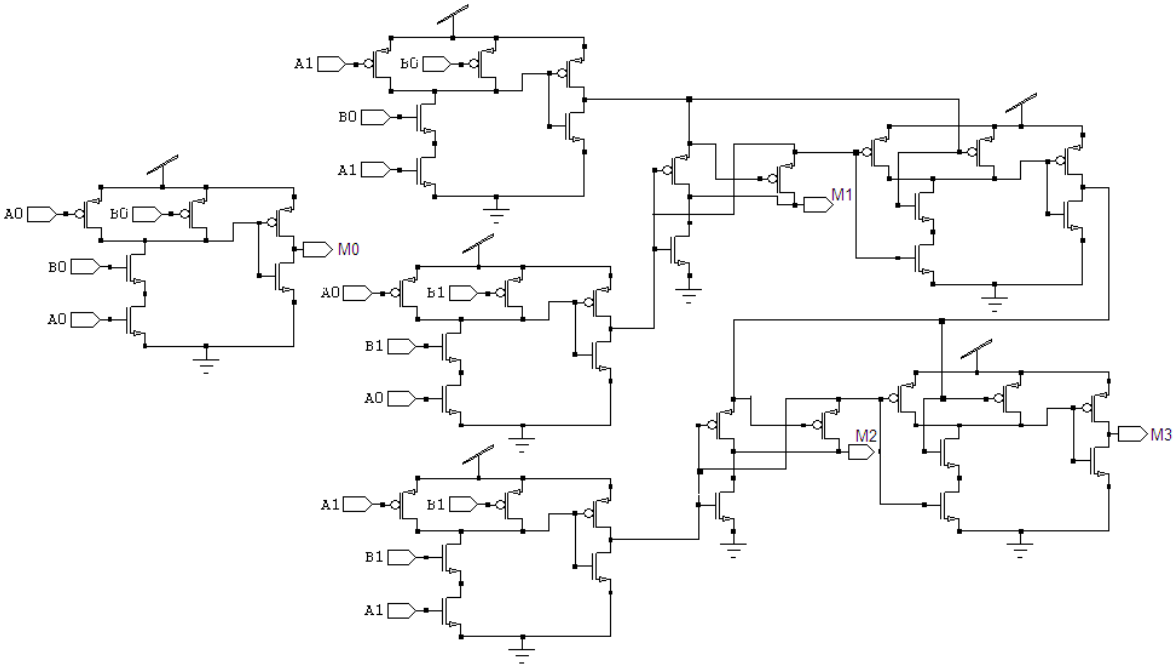

Figure 5. Schematic of 2×2 array multiplier using existing 3T XOR gate

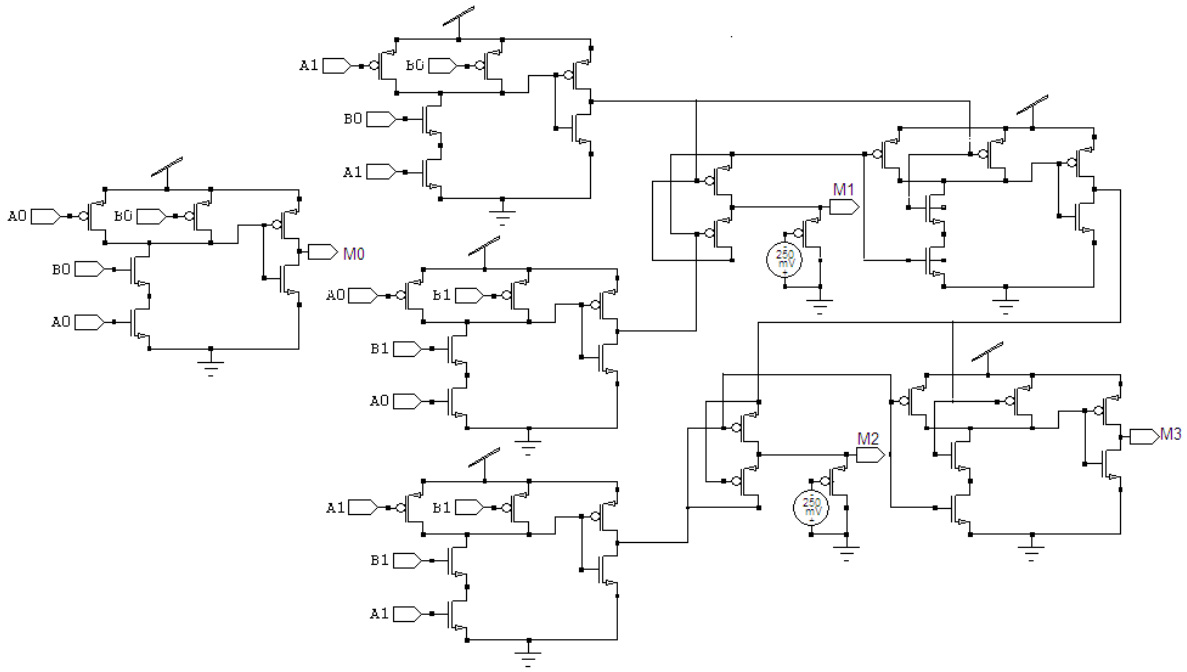

Figure 6. Schematic of 2×2 array multiplier using proposed 3T XOR gate

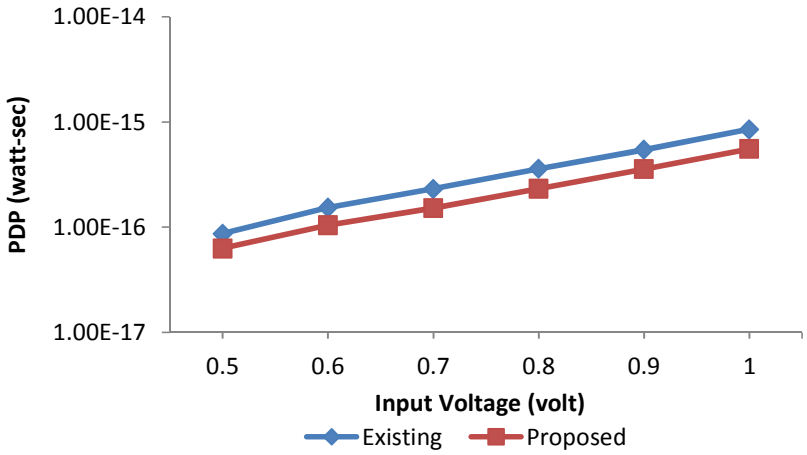

Figure 7. PDP consumption with increasing input voltage

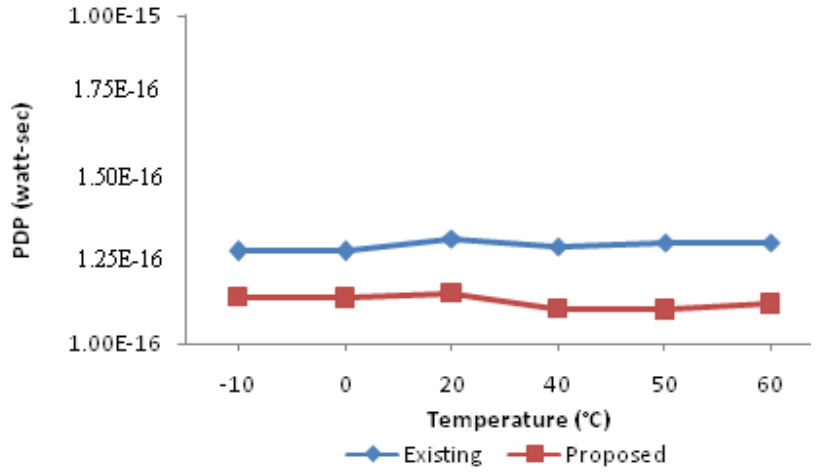

Figure 8. PDP consumption with increasing temperature

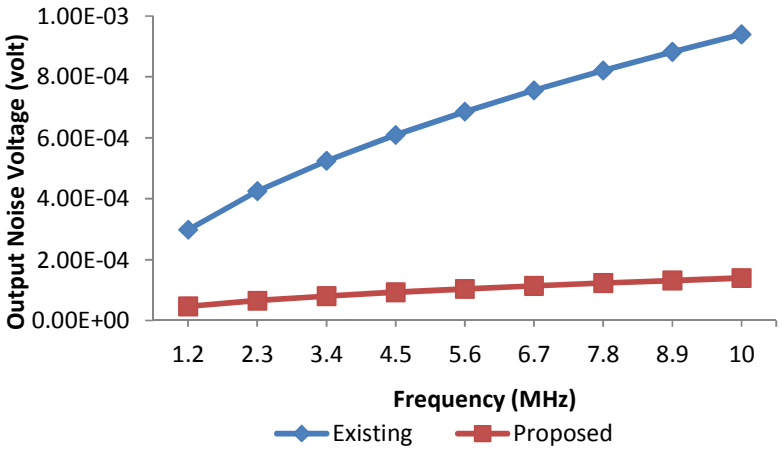

Figure 9. Output noise voltage with increasing operating frequency