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1-Bit Full Adder Circuit using XOR-XNOR Cells with Power and Area Optimization

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Abstract
This paper revel a realization of a superior circuit design of 1 bit full adder. The circuit is planned and implemented by using planar DG –MOSFETs at 45 nm technology. In CPU, arithmetic logic unit (ALU) is the core heart. The adder cell is the important and necessary unit of an ALU. In the present paper, an improved 1-bit full adder circuit is proposed that consumes lower power and reduced number of transistors. The proposed adder circuit consists of 9 transistors and called as 9-T adder cell. The planar DG-MOSFETs are new emerging transistors which can work n nanometer range and overcome the short channel effects. The simulation of proposed circuit is done in tanner tool version 13.0 using level 54 model files. The simulation is done to compare power, power delay product with supply voltage. The result is also checked at room temperature. This circuit performance of the proposed circuits compared with other reported circuits in literatures and it is seen approximately more than 99.9% reduction in power consumption.
Keywords: Low power; Area Efficent; Full Adder; GDI; Multiplexers

Introduction

The battery driven and portable devices are demand of current industry application which needs an implementation of low power and area efficient devices. According to Moore's law[1] doubling module concentration upon silicon wafer in each 3 years. The network of interconnection restricted circuit density on a chip, though transistor gate length is reduced to significant level. Today industrial applications are designed in 2 nm range. Microprocessors are fundamental and imperative part of many products that is required everyday such as radio, home appliances and computers systems. The size of transistor is restricted with phenomena short channel effects which include hot carrier effect, gate induced barrier lowering, DIBL effect and tunneling through oxide thickness. The degradation of device performance and device lifetime at smaller gate length is due to increased electric field. Transistors are the chief part of microprocessors. The foremost challenge in microscopic problems at nanometer range is ultra high speed; power dissipation and supply voltage. Lower power leads to lesser power supplies, less special batteries.

Further lowering of these resources will cut down the cost of overall system. In CPU, arithmetic logic unit (ALU) is the core heart. The adder cell is the important and necessary unit of an ALU. In the present paper, an improved 1-bit full adder circuit is proposed that consumes lower power and reduced number of transistors. The block diagram of full adder circuit is shown in Fig.1 (b).

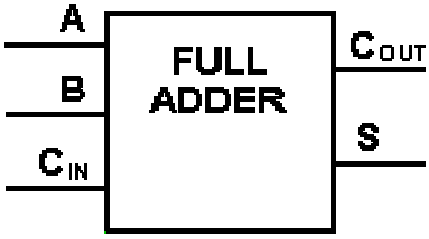

Fig.1(a) Block diagram of Full Adder

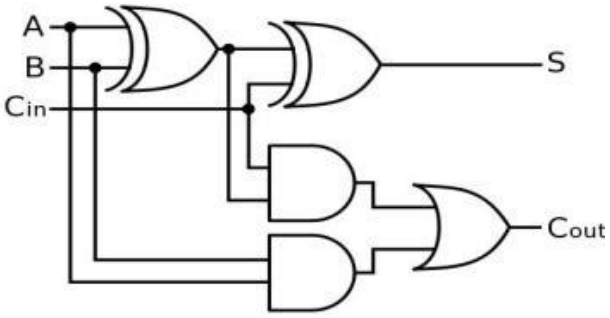

Fig.1(b) Single-bit Full Adder

There are two inputs as following a and b and the third input is called as an input carry as cin. The schematic circuit presentation of full adder is shown in Fig.1 Fig.1(b).the byte wide full adder and cascade carry bit from first adder to next is designed by use of 8 inputs. The output carry is designated as cout and the output is called as S. the truth table for 1 bit full adder is shown in table I.

Table I Truth table for full adder circuit

a	b	cin	sum	carrry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

RELATED WORK

There are number of circuits of full adder that has been designed owing to its importance in various electronic circuits. The full adder circuit is heart of many digital and analog circuits. It is used as major computing circuits for mainly digital designs. The analysis of full adder circuit is done for low power, reduced delay, and low power delay products. The circuit can be analyzed for different inputs as frequency, input voltage. It is given by Jin-Fa Lin, Yin-Tsung Hwang and Ming-Hwa Sheu in [6] that fast full adder circuit can be designed. XOR XNOR designed with PTL, module is used to implement fast full adder. Although circuit is fast and has low power consumption but outputs are degraded. This owes to PTL circuit technique which gives a threshold voltage loss in Nmos AND pMOS transistors. The circuit also shows noise due to threshold voltage loss in the gate circuit. Soolmaz Abbasalizadeh and Behjat Forouzandeh in [7] implemented a reliable and energy efficient full adder circuit cell. In this paper, they develop a consistent and energy proficient new adder cell with 11 transistors, it is on based GDI, transmission gates and pass-transistors for the low power. It is noticed that for all input arrangement there is no direct pathway from the supply voltage to the ground. It will eliminate the short circuit current. This circuit gives low power but again outputs are degraded. The delay of circuit is higher due to carry generating part. Ruchika, Tripti Sharma and K. G. Sharma in [8] designed another reliable and low power circuit of full adder. The use of sub threshold circuit designing in fast and energy efficient circuits is always needed in electronics. So for this proposed design sub threshold conduction is used. Two exclusive OR using 3T XOR gate are cascaded to obtain the sum output of three inputs. 2T multiplexer is used to implement the carry output. Because of better control on short channel effect, Double Gate MOSFET is used for sub threshold circuit design. DG-MOSFET is implemented using the equivalent system.

The two Single Gate MOSFET transistors are used to design DG MOSFET by connecting them in parallel in way that their source and drain are merged together. The Symmetrically Driven Double Gate and Independent Driven Double Gate MOSFET are two modes in which DG-MOSFETs are used to design digital and analog electronic circuits. The major difference between the two lies in the way the gates are biased. The front and back gates are linked together in DG MOSFET SDDG mode. The separate voltage are provided to the front and back gates to work in IDDG modes.

Richa Saraswat, Shyam Akashe and Shyam Babu in [9] provide a flexible and reliable DG MOSFET based full adder circuit. Double Gate is two independent gates which provide designer or researcher more power to design circuit with flexibility. Double Gate Field Effect Transistors are new alternative transistors which will reduce the Short Channel Effects (SCE) of nano scale devices because of their more electrostatic power over channel charges. In this paper, they propose a low power and area efficient full adder. 10 transistors based full adders shows a lower area of design as compare to full adder circuits which are implemented with higher no. of gate and also show significant reduction in power consumption and lower operating voltage. The reduction in voltage swing may be beneficial to power consumption. But it will slower switching for cascaded procedure in ripple carry adder. So there is no problem of degraded output. Noor Ain Kamsani, and Muhammad Faiz Bukhori [10] they have implemented a bridge style low power and very fast full adder circuit. This circuit has very low delay due to simultaneously working of all parts of full adder. The circuit uses a bridge style to implement full adder. In this circuit pass transistors based multiplexer is used. The necessary and important design constraint in circuit configuration is silicon wafer area, this design does not able to solve this problem but we can take tradeoffs between these constraints. This circuit has more transistors counts which will increase are and power consumption. The work is done at 130 nm. Anuj Kumar Shrivastava, Shyam Akashe[11] had proposed adder circuit which implemented with 4T XOR gate. XOR gate is regarded as the fundamental building block of full adder circuit. This proposed circuit behaves full adder and produces a addition operation. The power Gating

technique is reduce to the leakage current by adding NMOS and PAMOS to the circuit [12-13]. The main problem in this circuit is additional 2 transistors which are required to implement this technique. This will increase transistor count and as well as area of chip. Amit Kumar, Pankaj Srivastava, Manisha Pattanaik[14] in this paper have used body basing technique to implement the full adder circuit. Further semi-dominio technique is used to improve power performance of circuit. The full adder circuit is considered for low power and low complexity systems. Body biasing will decrease the threshold voltage which leads to low power designing of full adder circuit.

EXISTING FULL ADDER CIRCUIT DESIGN

The inspiration behind designing the lesser power full adder is to reveal that utilizing lower transistor count as a part of examination for ordinary adder, further the reduction in the propagation delay time and control utilization. It leads to diminishing the design range in reducing the overall chip size in circuit design in which this adder is utilized. The utilization of power is turning significant.

A. Gate Diffusion Input Technique GDI:

This technique is appropriate for lower delay and reduced power circuit design. This is because this technique can help to decrease the transistor count as compared to CMOS and other obtainable low power methods. by using GDI technique, the voltage swing and static power dissipation is also improved [17] this will improve overall performance of circuit. The fundamental unit of GDI is depicted in Fig.2 one nMOS and one pMOS together forms GDI MUX cell. The arrangement looks like a CMOS inverter. It has three input points: The output at D (in which NMOS and PMOS shorted drain terminal), G act as input(shorted NMOS and PMOS), P (PMOS source input), and N (NMOS source input). [18]. the three major reasons of power dissipation in CMOS VLSI circuits are short-circuit current, leakage current, Logic transition, [19], [20]. This technique avoids a short circuit between supply to ground terminal and this increases power utilization of proposed design [19].

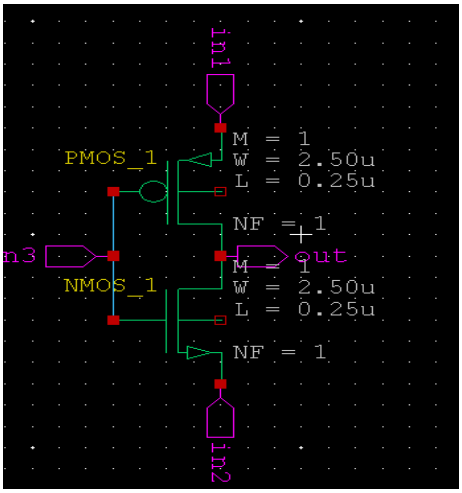

Fig. 2 2-T multiplexer

12-T full adder which is based on GDI based MUX, this circuit avoids a direct links in the between of supply and ground. This will reduce the short circuit current due to switching; i.e, the power utilization because of short out current is remarkably minute. In the proposed 12T full adder, all the select lines of the MUX i.e. the G nodes of the GDI cells are specifically joined with the data signals, comes about a much quicker move at output terminal . Therefore, the power consumption of the out stage is lower and overall power of system is reduced. the existing circuit require all 6 of 2T MUX based on GDI having same properties to propose a 12T full adder. The simulations are done using SPICE tool at 250 nanometer with usual level 54 model technology at room temperature; with input voltage of range of 1.5. The input and output waveforms show that this circuit works perfectly as full adder circuit and have very less degradation in outputs of this circuit. The average power consumption and pdp is 1.251488e-006 watts and 26.8 e-015 watt-sec respectively.

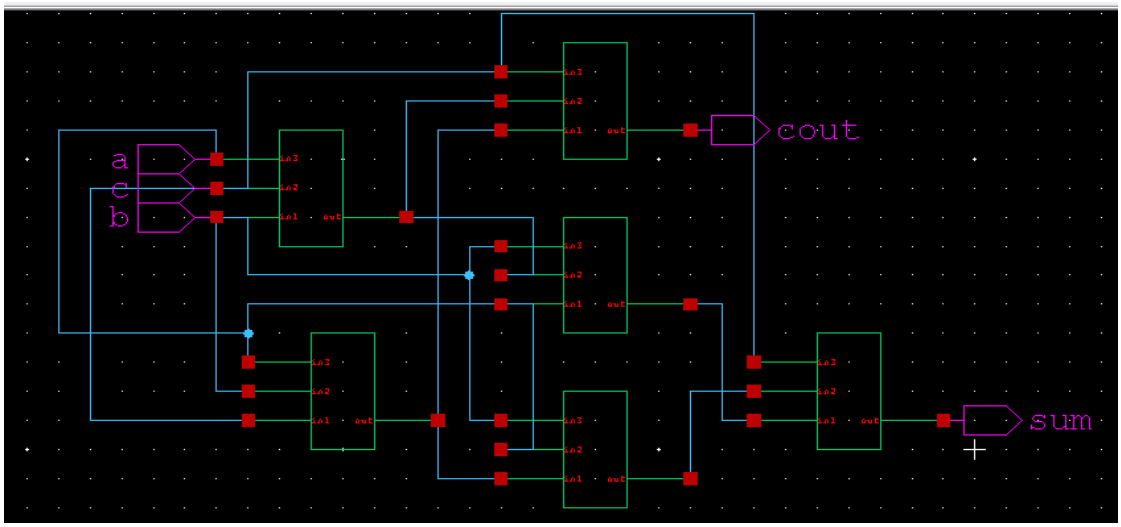

Fig.3 Schematic Design of Existing Full Adder

PROPOSED CIRCUIT

The working principle of proposed full adder design is shown below. The three inputs for 1-bit adder are *a*, *b*, and cin, the two 1-bit outputs are sum and cout. The sum and cout module are generated by following equations. The proposed circuit consists of 3T xor, 1 inverter and 2 multiplexers. There is difference for operating principle of this circuit is as compare to conventional circuits of full adder. The output at sum module in this circuit is generated as shown. The output is verified for input *A* = "0" and another for *A* = "1" as opposite to existing the conventional Sum module.

$$\text{sum} = a \oplus b \oplus \text{cin}, \quad (1)$$

$$\text{cout} = a \,.\, b + \text{cin}(a \oplus b) \quad (2)$$

The inputs *b* and cin are XORed and XNORed to produce sum module foe input a =0 and 1 respectively. The related equations are shown in (3) and (4). The logic for cout output is indicated in equation (5) and (6).

When $a = 0$,

$$\text{sum} = b \oplus \text{cin}. \quad (3)$$

When $a = 1$,

$$\text{sum} = b \odot \text{cin}. \quad (4)$$

For cout, when

$$b \oplus \text{cin} = 0, \text{cout} = \text{cin} \quad . \quad (5)$$

When $b \odot \text{cin} = 1$,

$$\text{cout} = a \quad (6)$$

XNOR logic output is produced by use of inverter which will invert the output of XOR module. Further 2T multiplexer is used to produce sum with a input as control voltage provided at gate terminal of 2T MUX. Another 2T multiplexer is used to generate cout which is controlled by XOR gate circuit and drives either *A* or Cin consequently at output of cout module. The proposed lowers the power delay product and also achieves better power supply compatiblity in sub threshold conduction region.

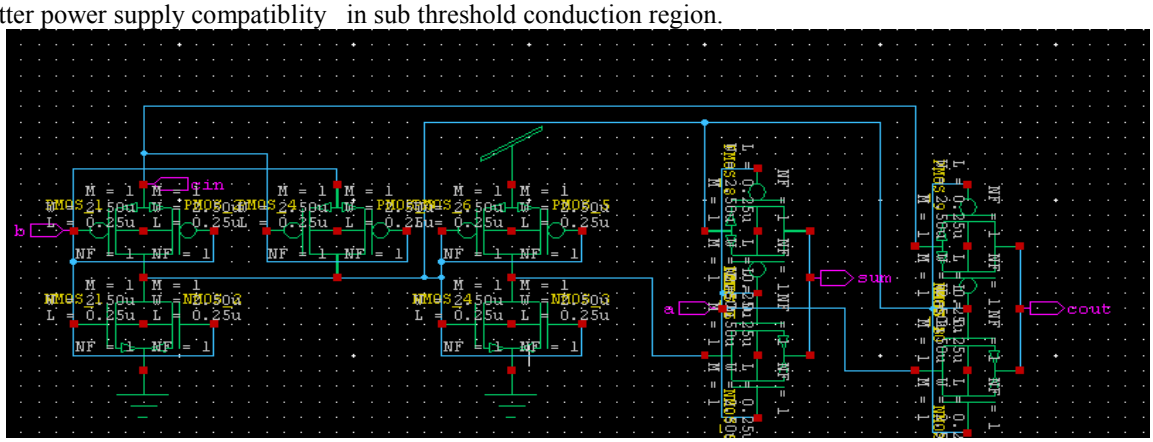

Fig. 4 Proposed circuit of planar DG MOSFET full adder circuit

Simulations Reseults

The transient analysis of proposed circuit is done for variety of input voltage in range at 45 nm. Fig.5 reveals an output waveform for time analysis. The parameters like frequency and temperature constant are kept fixed to analyze the performance of circuit for different input voltage and temperature for pdp and power consumption. The average power consumption and pdp is 8.98 nwatt and 101.5 x e^-18watt-sec respectively for proposed circuit as shown in Table II and III respectively.

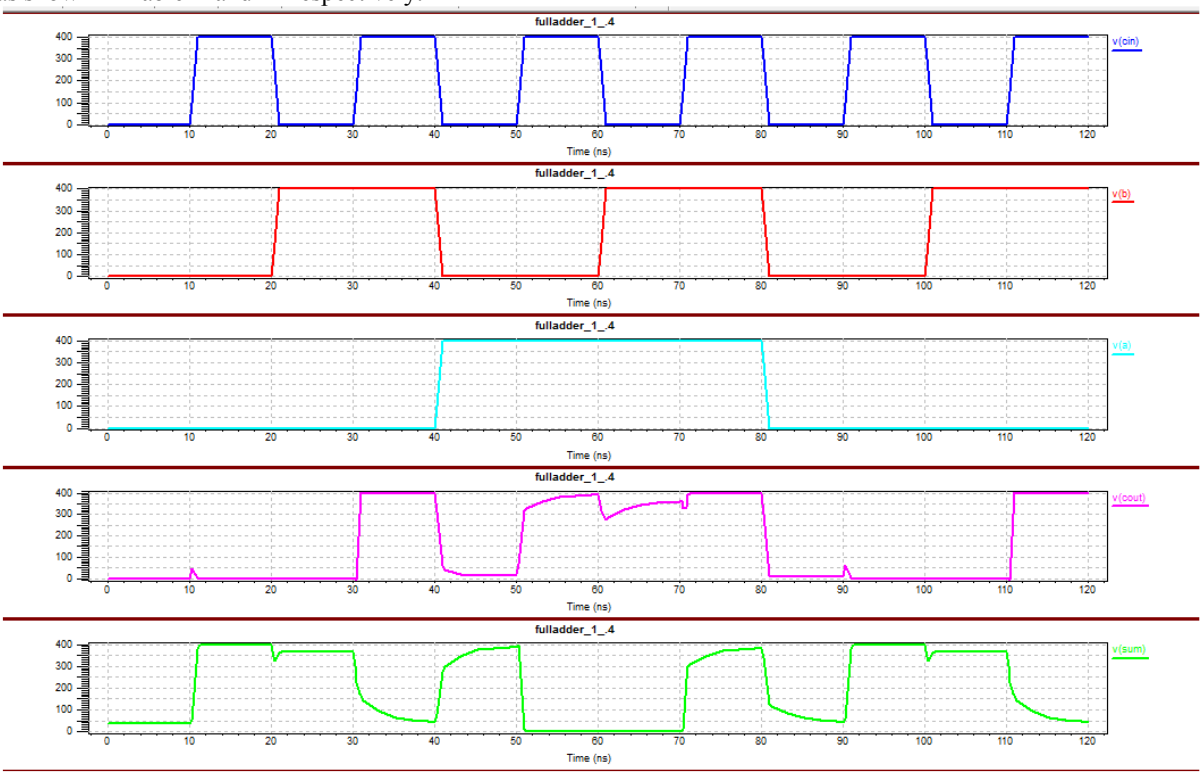

Fig. 5. Transient Analysis for existing full adder

Table I comparison of different parameters

Parameters	**Existing**	**Proposed**
input voltage(v)	1.5	0.50
power dissipation	1.25 e-006	9.2 e-009
power delay product	26.8 e-015 watt-sec	69.3e-18 watt-sec
technology(nm)	250	45
transistor count	12	9

Table II: power consumption with input voltage for proposed circuit

input voltage (v)	power consumption (w)
0.4	4.83e-009
0.45	7.08e-009
0.5	9.233e-009
0.55	14.8e-009

Table III: pdp with input voltage for proposed circuit

input voltage (in v)	power delay product (in e-18)
0.40	46.8
0.45	69.3
0.50	94.1
0.55	214.4

Conclusion

In this work, the proposed circuit is implemented by using the planar DG-MOSFET 1 bit full adder. This circuit attains reduced power and high. The double-gate (DG) or multigate devices provide a more power for reduction in gate length; hence it is useful for designing low power circuit in sub threshold conduction region. The study of different full adder circuits concludes appropriateness of DG MOSFETS for them. The proposed circuit is better than existing circuit is terms of power, area and no. of transistors

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