

MATLAB/SIMLINK Model for Three Phase Hybrid Multilevel Inverter Based on Half Bridge Modules

E.Madhana Gopal

PG student, Dept of EEE, RGM college of Engg and Technology, Nandyal, India
venkatmadhan243@gmail.com

M. Siva Shankar

Asst.professor, Dept. of EEE, RGM college of Engg and Technology Nandyal, India
kavi206@gmail.com

S. Ashwak hussain

Asst.professor, Dept. of EEE, RGM college of Engg and Technology Nandyal, India
aswak.hussain@gmail.com

Abstract

Nowadays the multilevel inverters are widely used in power electronic applications. The multilevel inverters are recommended for medium and high voltage applications. Multilevel inverters have become more popular due to reduced switching losses, low costs, low harmonic distortion and high voltage capability when compared to traditional PWM inverters. This paper deals with hybrid multilevel converter which is synthesis of neutral point clamped and cascaded multilevel inverter. The hybrid multilevel converter is proposed for medium voltage large power ratings. The proposed converter consisting of voltage source inverter connected with half bridge modules at each phase. With the proposed connection large portion of energy can be preceded by the VSI by connecting single multi pulse rectifier. The smaller power shares processed within the half bridge modules. The modulation scheme for hybrid multilevel inverter is naturally achieved by using logic circuit. The modulation scheme for four-level version is analyzed in detail for higher modulation (HM), three level version is analyzed for lower modulation (LM). This modulation scheme allows unidirectional power flow in all DC sources. For unidirectional application, the diode bridges are employed at rectification input side. The modulation schemes of sinusoidal pulse width modulation (SPWM), space vector PWM (SVPWM) are analyzed by using MATLAB/SIMLINK. The comparison of THD's for SPWM and SVPWM modulation techniques done by using MATLAB/SIMLINK.

Keywords: Hybrid Converters, Multilevel Converters, PWM Modulation, Three Phase Inverters.

I INTRODUCTION

In recent years industry has demanding high power equipment which now reach mega watt level multilevel converters are most widely used in power electronics for high voltage and high power applications. Multilevel converters are mainly utilized to synthesis a desired single or three phase voltage wave form. The desired multi-satire case output voltage is obtained by combining separate dc sources. Multilevel inverter is designed by more number of switches to obtained stair case output. the multilevel inverters are mostly used in power electronic applications like power quality, power system control, adjustable speed drives uninterruptable power supplies (UPS).in the industrial applications mostly three phase multilevel inverters are used.

Nowadays, there exists three types of multilevel voltage source inverters namely neutral point clamped inverter (NPC), flying capacitors (FC's), cascaded H bridge inverter (CHB). Among these multilevel inverter cascaded multilevel inverter is reaches the higher voltage and high power levels. By increasing voltage levels the number of switches will increase which leads increasing swathing losses.[1]-[12]

Diode clamped converter also known as neutral point clamped inverter (NPC). [19],[20] which is widely used in three phase power conversion. There is a single dc link spit in to two or more equal voltages which clamp the main voltage of main switches through fast switching diodes. This is used in high power ac drive applications like conveyers, pumps, fans in mining, Marian, gas, oil industries. The capacitor clamped converter also known as flying capacitor converter. The flying capacitor converters are used in high band width high frequency applications.[17]-[18]

Finally, cascaded multi level inverter has been applied in high voltage, power essential conditions. This cascaded multilevel inverter employs dc side isolated series connected full bridges allows high modularity less number of switches as compared to NPC, FC. Cascaded half bridge converters employs series connected half bridge modules instead of full bridge ones. This converter is alternate to the full bridge ones. The modular multilevel converter provided of series connected pair of half bridge modules.[16]

operating stages for phase A of proposed converter is show in Fig .3. the output voltage v_A can be obtained in six different levels. The output voltages can be obtained for three phases as v_o with $o=A, B, C$. shown in table I. the output voltage is depends on dc source voltages V_x and V_y on the switching states of S_{j0} and $S_{j0'}$,with 1, 2,3. Based on these results, the HC1/2B the number of levels N varying from four to six given that

$$f(x) = \begin{cases} 4 & \text{if } V_x = V_y \\ 5, & \text{if } V_x = V_y/2 \\ 6 & \text{if } V_x \neq V_y \neq V_y/2 \end{cases} \quad (1)$$

Based on the switching states the phase voltage levels can be obtained is given in Table I. for four level HC1/2B symmetrical dc source the space vectors are shown in Fig 4(a) with .

The resulting state space is composition of VSI spaces and pair of half bridge spaces. For asymmetrical case the space vector space is shown in Fig 4(c). to generate phase voltage in converter it is not necessary to switch the VSI state but half bridge spaces are generate voltage spaces in converter. That relatively increasing dc voltage for VSI expands VSI space and creates higher number of levels. The voltage rating for semiconductor is change by space vector space.

Switching stages for hybrid multilevel converter with single phase leg are

- (a) $S_{1A'}$, $S_{2A'}$ and S_{3A} are on and ;
- (b) S_{1A} , $S_{2A'}$ and S_{3A} are on and ;
- (c) $S_{1A'}$, S_{2A} and S_{3A} are on and ;
- (d) S_{1A} , S_{2A} and S_{3A} are on and ;

The output voltage referred as virtual reference shown in centre point of source

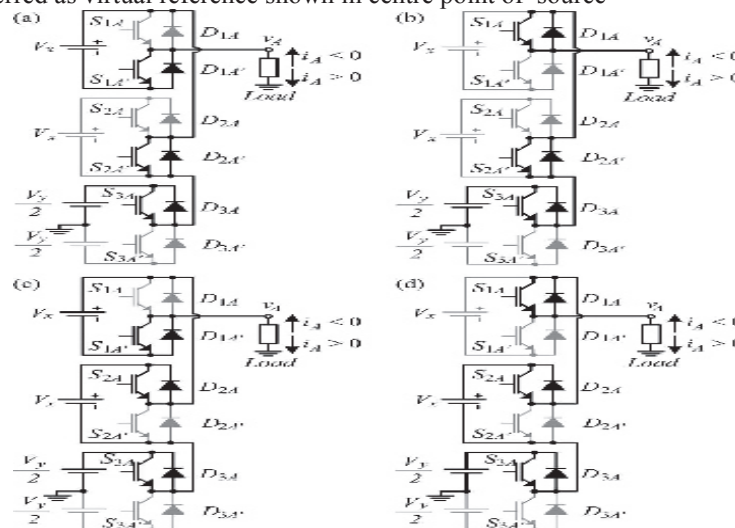


Fig 3 operation stages for phase leg of proposed multilevel converter employing half bridge modules for positive output voltage

TABLE I
 RESULTANT OUTPUT PHASE VOLTAGE (V_o , WITH $o=A,B,C$)AS A FUNCTION OF SWITCHING STATES AND OF THE DC SOURCE VALUES V_x AND V_y WHERE $S_{jo}(j = 1,2,3)$ CORRESPONDS TO THE STATE OF SWITCH S_{jo} AND $S_{jo'}$ (SWITCH ON ;1,SWITCH OFF ; 0)

S_{10}	S_{20}	S_{30}	V_o	Case 1 $V_x = V_y = V_{cc}$	Case 2 $V_x = \frac{V_y}{2} = V_{cc}$	Case 3 $V_x = \frac{V_y}{3} = V_{cc}$
0	0	0	$-V_x - V_y/2$	$-3V_{cc}/2$	$-2V_{cc}$	$-5V_{cc}/2$
1	0	0	$-V_y/2$	$-V_{cc}/2$	$-V_{cc}$	$-3V_{cc}/2$
0	1	0	$-V_y/2V_x - V_y/2$	$-V_{cc}/2$	$-V_{cc}$	$-3V_{cc}/2$
1	1	0		$V_{cc}/2$	0	$-V_{cc}/2$
0	0	1	$-V_x + V_y/2$	$-V_{cc}/2$	0	$V_{cc}/2$
1	0	1	$V_y/2$	$V_{cc}/2$	V_{cc}	$3V_{cc}/2$
0	1	1	$V_y/2$	$V_{cc}/2$	V_{cc}	$3V_{cc}/2$
1	1	1	$V_x + V_y/2$	$3V_{cc}/2$	$2V_{cc}$	$5V_{cc}/2$

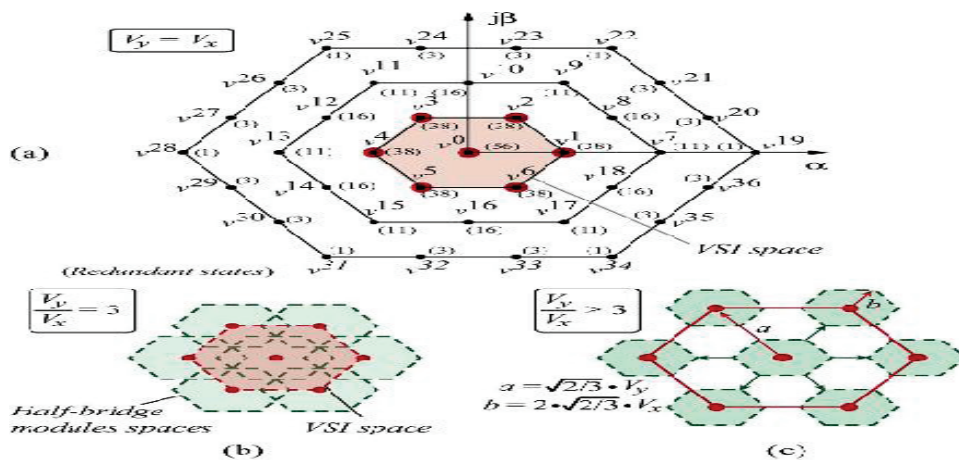


Fig 4space vectors for proposed converter (a)space vectors for four level converter employing;(b) contributions for modulation domain for ,and (c) contribution for modulation domain .

IV MODULATION SCHEME FOR FOUR-LEVEL CONVERTER

This section presents the modulation scheme for four level operation of HC1/2B. In this converter the switches of the three-phase VSI at low frequency transfer the switching losses to half bridge modules. This feature allows to use low speed switches in three phase inverter reducing conduction losses in VSI. While keeping the switching losses at same level, the losses shifted to half bridge modules. The non uniform distribution of switching losses occur, the modulation scheme is able to distribute losses among the half bridge modules. By switching the switches and with $\alpha=A, B, C$ and $j=1, 2, 3$ in complementary way. For the generation of three phase VSI switching signals we develop demand logic. Thus this modulation strategy is known as hybrid modulation. As it used high modulation indexes it is named as HM. the half bride modules are derived by comparing sin modulating signal Ref_j to three synchronous triangular carrier Car_j , as shown in Fig 5(a).

Uncontrolled rectifiers can be employed for unidirectional power flow applications by connecting all dc sources. The positive and negative power flow shown in Table II at some of insulated dc sources does not depend only on the switching states but also on direction of phase currents. The modulation pattern previously described is not able to guarantee unidirectional power flow in dc sources for the half bridge modules for

modulation index ranging from null to unity.

The output voltages of VSI are kept constant during each half period and this force the half bridge modules process more power and regenerate it to the source of low modulation indexes. It is clearly observed in Fig 6 the power flow at insulated dc source become negative for $M < 0.42$ and active power handled by all dc sources extremely high at low modulation indexes when compared to total active power transferred to load.

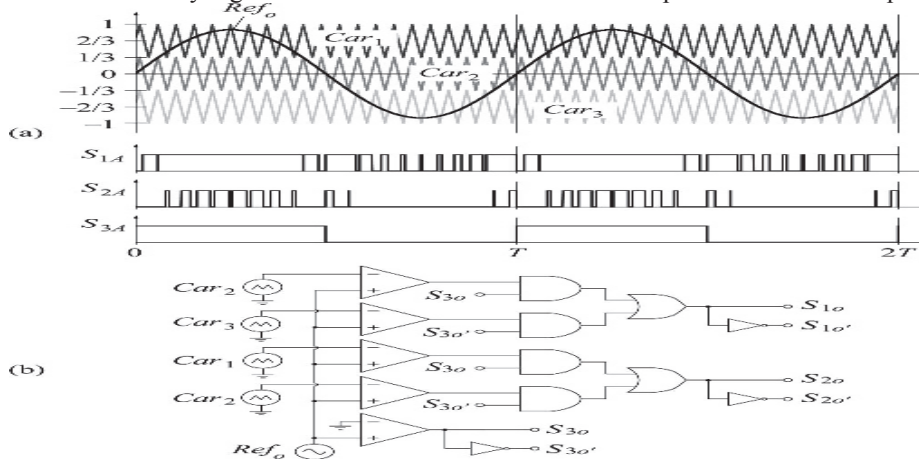


Fig.5.Modulation strategy HM: (a) timing diagram for four level operation and (b) PWM generation logic

Output phase voltage ($\phi = a, b, c$) and active power direction at the dc sources as a function of switching states, and output currents direction. ϕ and ψ are the average power proceeded by upper and lower dc sources respectively. Feeding the half bridge modules at phase ϕ , the plus signal (+) indicates that the source is feeding power. the minus signal indicates that the source is sinking power .the empty signal (\emptyset) indicates that no current flow in the source.

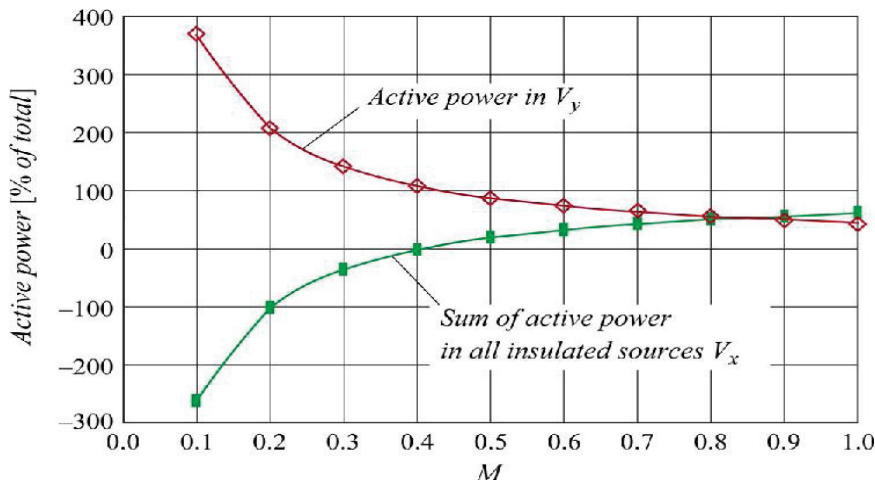


Fig 6. Active power handle by dc sources as a percent of the total load power total modulation pattern HM

One way to avoid the regenerative power flow in the insulated dc source is to switch the three phase VSI at high frequency .generating output PWM voltages with sinusoidal behavior proportional to modulation index. Switching losses at the VSI would increase accordingly. So the modification of modulation logic proposed. The VSI high side are low side switches are turned on during whole period when $M < 1/2$.the modulation pattern $M < 1/2$ is shown in Fig 7 termed as modulation LM.

The modulation scheme basic algorithm is as follows.

- $0 \leq M \leq 1/2$ (LM) : the VSI has all switches either clamped to the positive or negative rail. The clamping can be changed at every modulation cycle to balance the losses at all semiconductors or, whenever possible a bypass mechanical switch can be driven to reduce conduction losses. The half bridge process all the active power transferred to the load
- $M > 1/2$ (HM) : the each VSI leg switches a single per modulation period and half bridge modules handle a smaller power share. This modulation scheme is able to generate three phase sinusoidal PWM modulated voltages at any modulation index. It presents the advantage of processing large power levels by three-phase VSI.

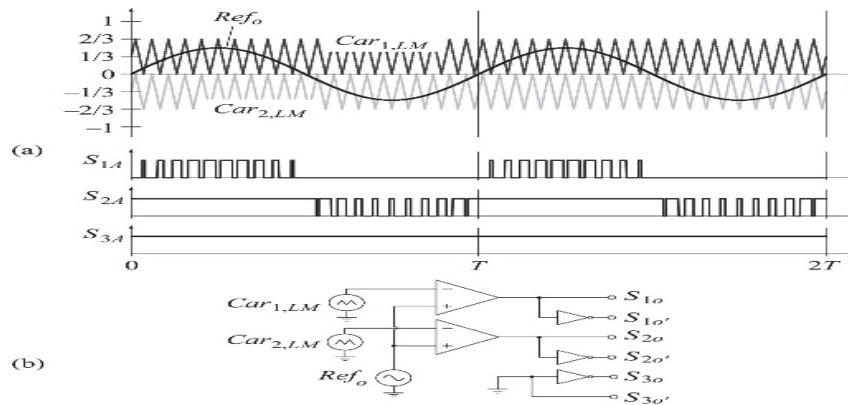


Fig 7: Modulation strategy LM: (a) timing diagram for three-level operation (b) PWM generation logic. Both LM and HM modulation patterns are able to produce line to line voltages with five level while all dc sources supply positive active power for range $4/(3\pi) < M < 2/3$. therefore, any modulation index with in this range can be achieved and a control can be used to switch between two methods without resulting in oscillations.

V. OUTPUT VOLTAGE ANALYSIS

The output voltage analysis for four level HC1/2B employing proposed modulation and consists in expressing output phase voltage as function of harmonic components of fundamental and carrier frequencies.

The inverter phase voltage can be expressed by

$$\begin{aligned}
 f(t) = & \frac{A_{oo}}{2} + \sum_{n=1}^{\infty} [A_{on} \cos(n.y) + B_{on} \sin(n.y)] \\
 & + \sum_{m=1}^{\infty} [A_{mo} \cos(m.x) + B_{mo} \sin(m.x)] \\
 & + \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ (n \neq 0)}}^{\infty} [A_{mn} \cos(m.x + n.y) + B_{mn} \sin(m.x + n.y)] \quad (2)
 \end{aligned}$$

With $x = \omega_c t + \theta_c$ and $y = \omega_o t + \theta_o$

In (2) variables x and y represents angular carrier frequency and the angular fundamental frequency, respectively, and the terms A_{mn} and B_{mn} express the amplitude of each harmonic component. The harmonic components are obtained by double Fourier integral

$$\begin{aligned}
 C_{mn} &= A_{mn} + B_{mn} \\
 &= \frac{1}{2} \cdot \pi^2 \iint_{-\pi}^{\pi} f(x, y) \cdot e^{j(mx+ny)} dx \cdot dy \quad (3)
 \end{aligned}$$

Where C_{mn} is the output phase voltage synthesized by the inverter

VI SIMULATION OF HYBRID MULTILEVEL CONVERTER

(A) SIMULATION BASED ON SPWM

Simulation of hybrid converter for four-level with IGBT switches shown in Fig 1. in this simulation model three phase rectifiers are connected with three phase transformers. The three phase diode bridge rectifies the voltage in secondary side of transformers and electrolytic capacitors smooth the dc voltage with low ripple. The total nine half bridge modules implement the four-level converter. The dc side input voltage is 580V and switching frequency of half bridge converter is 1kHz while output fundamental frequency is 50Hz. The execution of both modulation patterns LM and HM is performed in SIMLINK. the sinusoidal reference signals are displaced by 120° and a zero crossing detector is virtually executed to compare the polarity of sinusoidal references. the modulation patterns generated by given logic are observed in Fig 8

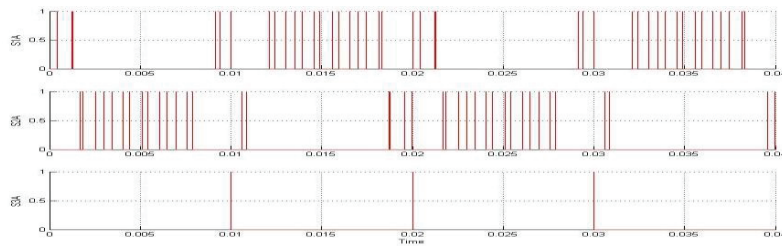


Fig.8 (a) implemented gate signal patterns for HM modulation

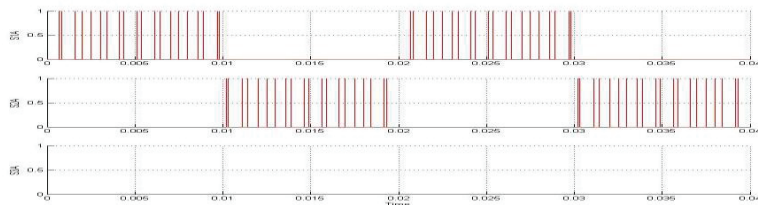


Fig.8 (b).implemented gate signal pattern for LM modulation

The command signals generated for both modulation patterns (HM and LM) based on SPWM technique are shown in Fig. 8. In Fig 8(a) the command signals for HM strategy and a modulation index $M=0.9$ are presented, while Fig. 8(b) shows the gate command signals for LM modulation for modulation index $M=0.5$.

By applying modulation index $M=0.9$ leads to phase voltages, i.e., voltages between load terminals and mid-point of VSI's dc-link, as shown in Fig.9. Fig 9 presents voltages it is observed that the phase voltages closely follow the simulated patterns and are displaced by each other. The measured line voltage is given in Fig. 9. the waveforms verify the theoretical analysis of seven level line voltage with low harmonic distortion.

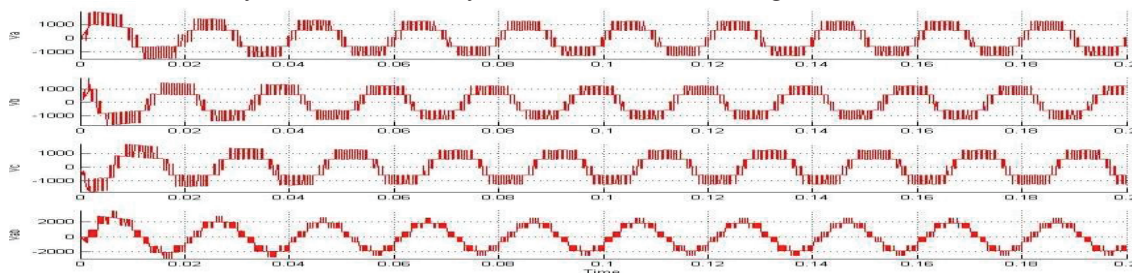


Fig.9. simulated results for $M=0.9$ and -HM modulation. Phase voltages at A, B, C and line voltage

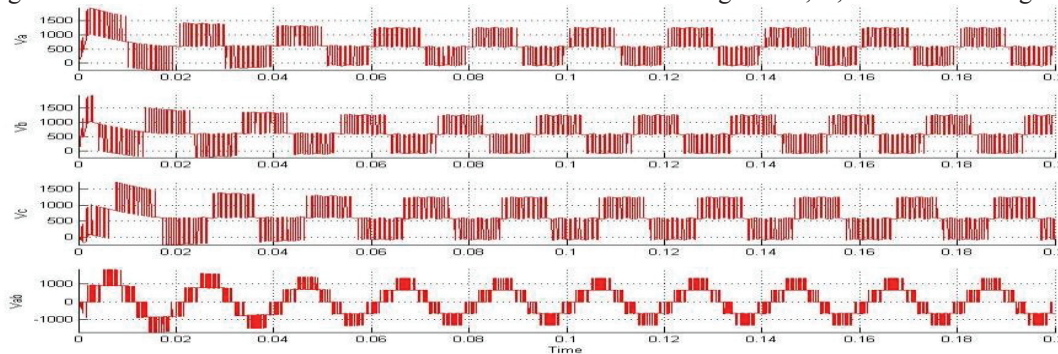


Fig.10. simulated results for $M=0.5$ and -LM modulation. Phase voltages at A, B, C and line voltage

By applying a modulation index $M=0.5$ shows the phase voltages in Fig.11. it is observed that the three level phase voltage follows the theoretical LM modulation pattern with dc offset due to measurement from the phase point to the centre point of the VSI's dc-link. the line voltage is shown in Fig.10

The modulation index has been varied from close to unity to close to null to verify active power distribution between insulated dc sources and to measure the THD line and phase voltages. The HM modulation pattern employed from $M=1$ down to $M=0.5$, while the LM was used for lower modulation index values.

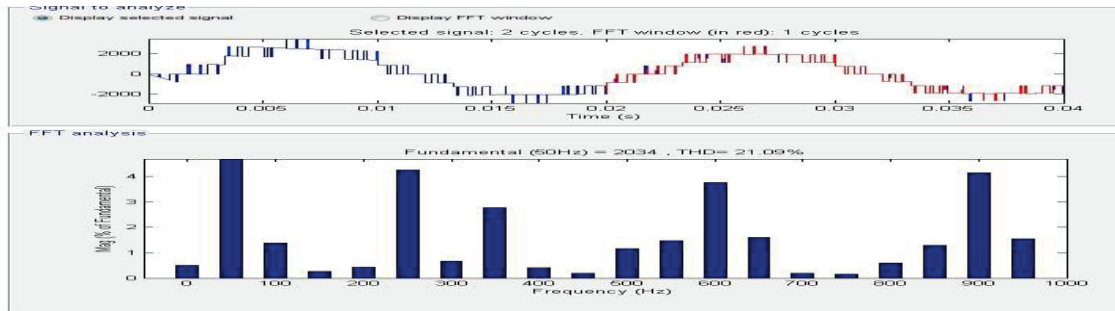


Fig. 11(a) the THD analysis for line voltage for HM

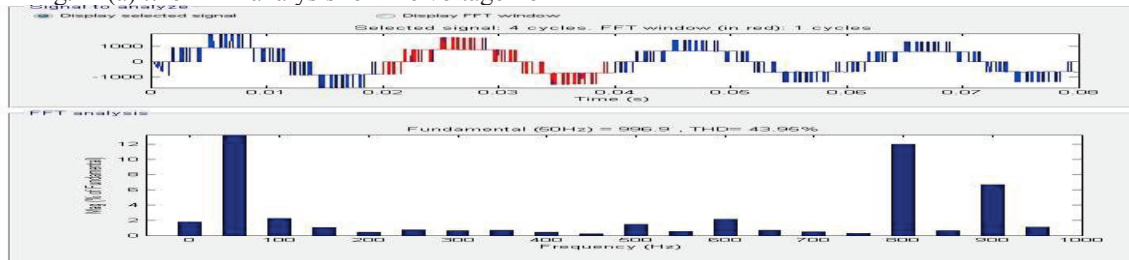


Fig 11 (b). The THD analysis for line voltage for LM

(B) SIMULATION BASED ON SVPWM

In the simulation of both HM and LM modulation technique the modulating wave is generated in SVPWM technique. The total circuit is as same as SPWM technique. the hybrid multilevel inverter circuit consist of six half bridges and one three phase VSI driven by pattern of SVPWM modulating waves.

The SVPWM technique generated voltage waveforms having low THD as compared to SPWM.

For the modulation index $M=0.9$ leads to phase voltages, i.e., voltage between load terminals A,B,C and mid-point of the VSI,s dc link, as shown in Fig 13.the SVPWM simulated HM and LM modulation pulses are shown in Fig 12.the SVPWM HM modulation phase and line voltages have low THD as compared to LM modulation.

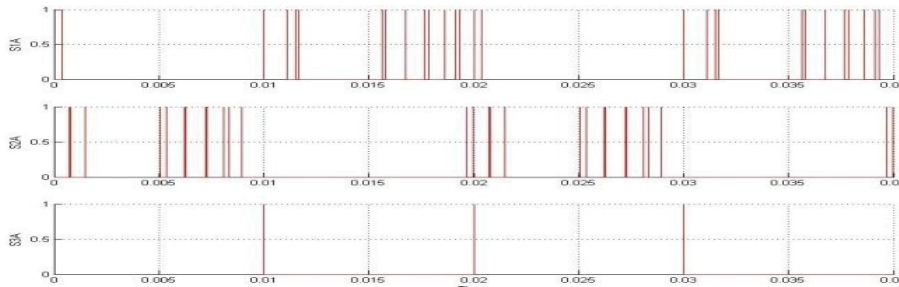


Fig 12(a) the simulated SVPWM gate signal pattern for HM modulation index $M=0.9$

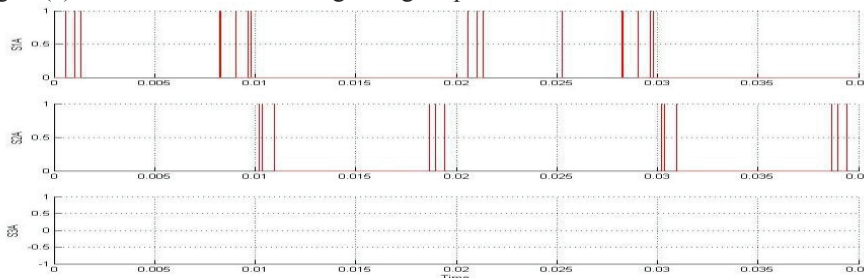


Fig 12(b) the simulated SVPWM gate signal pattern for LM modulation index $M=0.5$

By applying modulation patterns to the proposed converter it is observed that four level phase voltage follows by the HM modulation three level phase voltages follows by LM modulation pattern with dc off set due to measurement from phase terminals to centre point of the VSI's dc-link. The line voltage presents seven and five levels for HM and LM respectively

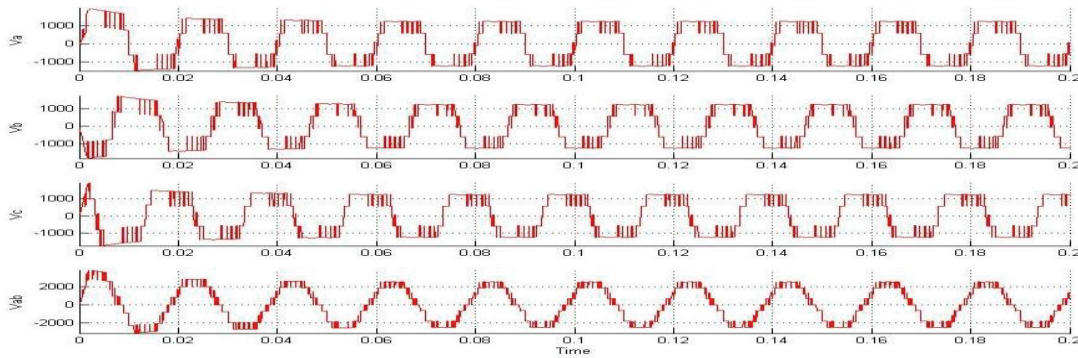


Fig.13. simulated results for $M=0.9$ and -HM modulation. Phase voltages at A, B, C and line voltage

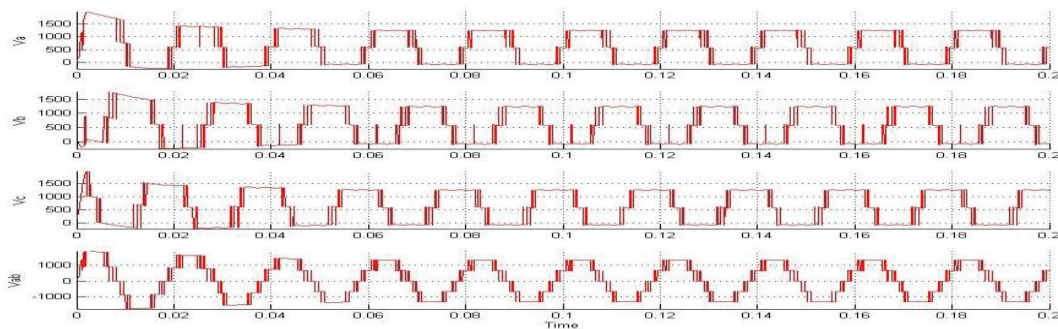


Fig 14. Simulated results for $M=0.5$ and -LM modulation. Phase voltages at A, B, C and line voltage

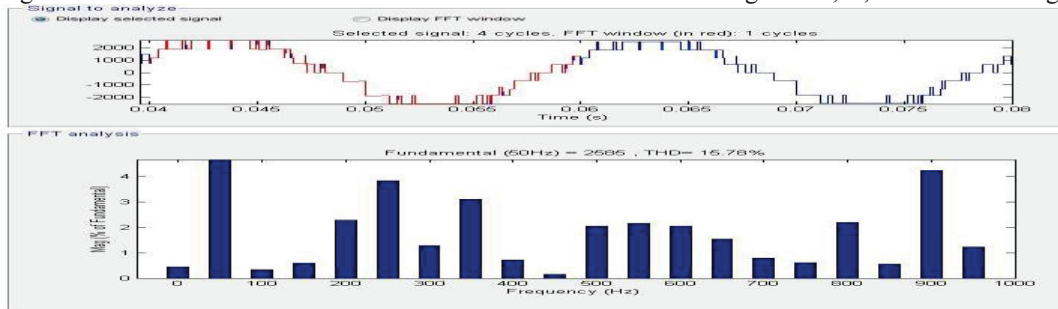


Fig. 15(a) .the THD analysis for line voltage for HM

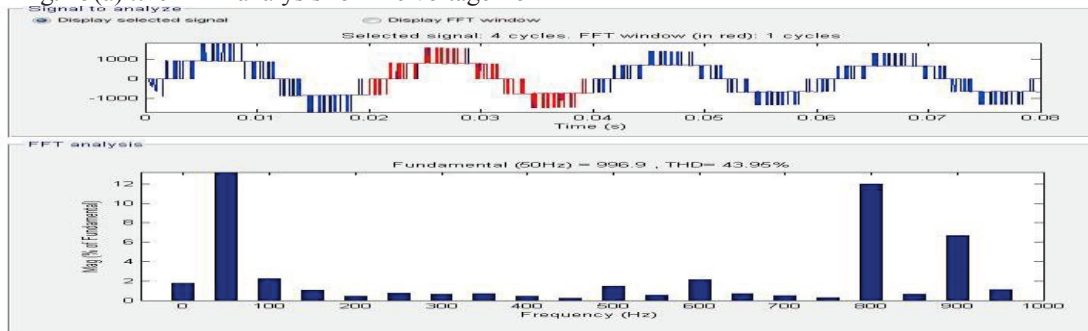


Fig. 15(b) .the THD analysis for line voltage for LM

The modulation index is varied from zero to unity. The total harmonic distortion varied based on modulation index .the measurement results are summarized as shown in Fig.16.

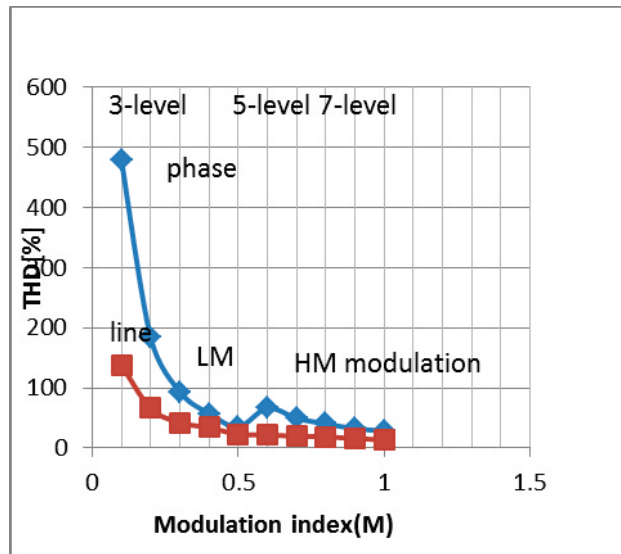


Fig 16. THD for line and phase voltages according to modulation index M

VII CONCLUSION

The hybrid multilevel converter is able to achieve three level and four level operations for HM and LM modulation. The main advantage of this solution is possibility of reduction of power rating for insulated dc sources. A four level hybrid modulation scheme has been presented, which allows unidirectional power flow in all dc sources for any modulation index and lower the power demand on insulated dc sources for higher modulation indexes. The theoretical analysis of output voltage has been presented and verified for LM and HM modulation of SPWM and SVPWM techniques. The phase and line voltage's with low THD's for SPWM and SVPWM techniques has been compared using SIMLINK.

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Mr. E. Madhana Gopal was born in Banaganapalle, India in 1989. He received B.Tech (Electrical and Electronics Engineering) degree from JNT University, Ananthapur in 2010, and pursuing M.Tech (Power Electronics) in RGM Engineering College(Autonomous), Nandyal. His area of interests are Power electronics converters, and Electrical Machines



Mr. M SIVA SANKAR was born in 1983. He received his Diploma in Electrical & Electronics Engineering from S.B.T.E.T., Hyderabad in the year 2003. He Graduated in Electrical & Electronics Engineering from J.N.T.U.H.,



Mr. S. Aswak Hussain is a Asst Professor in the Department of Electrical & Electronics Engineering RGM Engineering College (Autonomous),Nandyal.

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