The Use of Operational Amplifier in Providing Safety for Electronic Devices

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Abstract
Operational amplifiers find a wide application and usage in electronics, control and instrumentation circuits. This paper discusses the use of operational amplifier commonly referred to as Op-Amp in ensuring the longevity of electronic systems. Devices such as automatic voltage regulators, automatic inverter systems and so on make use of OP-Amp to provide safety for the system and other components that make up the device. In this work, the Op-Amp is used to provide overload and no load indication. A low and high battery level indication when in use and while undergoing charging process is ensured respectively; this however elongates the life-span of the battery. With the aid of an external shutdown circuit arrangement, the entire system can be shut down after given a prior warning alarm.
Keywords: Op-Amp, battery, Electronic Devices, Inverter.

1. Introduction

An operational amplifier ("OP-Amp") is a DC-coupled high-gain electronic voltage amplifier with a differential input, and usually, a single ended output. An OP-Amp produces an output voltage that is typically hundreds of thousands times larger than the voltage difference between its input terminals (Horowitz and Hill, 1989). Operational amplifiers are important building blocks for a wide range of electronic circuits. They had their origins in analog computers where they were used in many linear, non linear and frequency-dependent circuits. Their popularity in circuit design largely stems from the fact that characteristics of the final Op-Amp circuits with negative feedback (such as their gain) are set by external components with little dependence on temperature changes and manufacturing variations in the Op-Amp itself.

Op-Amps are among the most widely used electronic devices today, being used in a vast array of consumer, industrial, and scientific devices. The Op-Amp is one type of differential amplifier. Other types of differential amplifier include the instrumentation amplifier (usually built from three Op-Amps), the isolation amplifier (similar to the instrumentation amplifier, but with tolerance to common-mode voltages, and negative feedback amplifier) usually built from one or more Op-Amps and a resistive feedback network (Malmstadt, 1981, Stout, 1976). A standard Op-Amp has a minimum of five pins for its operation; this is shown in figure 1. The basic pins are: V_+ (non-inverting input), V_- (inverting input), and V_{out} (output), V_{S+} (positive power supply and V_{S-} (negative power supply)

The amplifier's differential inputs consist of a V_+ input and a V_- input, and ideally the Op-Amp amplifies only the difference in voltage between the two, which is called the differential input voltage. The output voltage of the op-amp is given as;

$$V_{out} = (V_+ - V_-) A_{OL}$$

Where V_+ is the voltage at the non-inverting terminal, V_- is the voltage at the inverting terminal and A_{OL} is the open-loop gain of the amplifier (the term "open-loop" refers to the absence of a feedback loop from the output to the input). Without negative feedback, and perhaps with positive feedback for regeneration, an Op-Amp acts as a comparator (Phillip and Douglas, 2002).

2. Discussion

2.1. *Op-Amp as a Comparator*

In electronics, a comparator is a device that compares two voltages or currents and switches its output to indicate which is larger. They are commonly used in devices such as analog-to-digital converters (ADCs), relaxation oscillator, null detectors, zero-crossing detectors, level shifter and so on. In theory, a standard op-amp operating in open-loop configuration (without negative feedback) may be used as a low-performance comparator (Jung, 2004). When the non-inverting input (V_+) is at a higher voltage than the inverting input (V_-), the high gain of the op-amp causes the output to saturate at the highest positive voltage it can withstand. When the non-inverting input (V_+) drops below the inverting input (V_-), the output saturates at the most negative voltage it can withstand. The Op-Amp's output voltage is limited by the supply voltage.

A dedicated voltage comparator will generally be faster than a general-purpose operational amplifier

pressed into service as a comparator. A dedicated voltage comparator may also contain additional features such as an accurate, internal voltage reference, an adjustable hysteresis and a clock gated input (Stout, 1976). A dedicated voltage comparator chip such as LM339 and LM324 is designed to interface with a digital logic interface (to a TTL or a CMOS). The output is a binary state often used to interface real world signals to digital circuit. Operational Amplifier plays a big role in the Pulse Width Modulated (PWM) based inverter system; the Op-Amp is used as a comparator in the inverter circuit. In this design, Op-Amp LM324 is used as a voltage comparator in the inverter circuit. The LM 324N is a quad two input Op-Amp. Four different Op-Amps in the LM324N can be used for four different works. Each of the Op-Amps in the LM324N IC package has three pins; two for input and one for output. Out of the two input pins, one is called inverting (-) input and the other is called non-inverting (+) input.

2.1.1. *Inverting Input (-)*

If the input given to this pin is less than the input given to the non-inverting input pin, then the Op-Amp output will be high. If the input given to this pin is more than the input given to the non-inverting input pin, then the output of the Op-Amp will be low. The output will be reverse of the input at the inverting pin; that is, if the input to the inverting pin is low, the output will be high and vice versa (Manahar, 2004).

2.1.2. *Non-Inverting Input (+)*

If the input given to this pin is less than the input given to the inverting input pin, then the Op-Amp output will be low. If the input given to this pin is more than the input given to the inverting input pin, then the Op-Amp output will be high. In summary, if the input to the non-inverting pin is low, the output will be low and if the input is high, the output will be high.

It can therefore be seen that the Op-Amp output depends on the value of the signal at its input pins. This property of the Op-Amp makes it useful as a comparator in inverter circuit (Rogenmoser, 1997). Op-Amps in the inverter receive a fixed reference voltage at its one input pin and the other input pin is given the value to be checked. When the value to be checked differ from the reference voltage, the Op-Amp output will go low or high. This output is used to provide audio/visual indication about the conditions of the protective circuit or to shutdown the inverter. In this paper, Op-Amp is used to provide safety for an inverter system; this is achieved by using Op-Amp to design a no load indication circuit, a low battery indicator circuit and an overload detection circuit. With the Op-Amp circuit arrangement, a visual indication is given when any of the conditions earlier mentioned is detected and with an external shutdown arrangement; the inverter system can be shut down after given a prior warning alarm about all the conditions given above.

3. Shut down System of an Op Amp

3.1. "No Load" Shut Down section

When the inverter is working in battery mode and no load is connected at the inverter output, or if the load at its output is switched off, the inverter senses this and automatically switches off itself. This type of protective circuit as shown in figure 2 is essential to protect the inverter from unnecessarily discharging the battery.

3.1.1 *How the "No load" is sensed*

Source (S) of the MOSFETs at the inverter output is grounded through a shunt. According to Manahar 2004, different polarity of 0V is generated at this shunt, based on the load connected to the inverter output. When no load is connected at the inverter output, the shunt shows negative 0V, and when proper load is connected to the output, the shunt shows positive 0V. The negative 0V is used by the no-load shutdown circuit.

3.1.2 *"No Load" Shutdown Circuit.*

The No-load shutdown section uses two Op-Amps using Pin-1, 2, 3, and 8, 9, 10 of IC1, transistors T3 and T4. Pin-2, 3, 9 and 10 are input pins of Op-Amp while Pin-1 and 8 are output pins.

3.1.3 *Working Principle of "No Load" Shutdown Circuit*

Pin-3 of IC1 receives positive 0V, through R12. Pin-2 of IC1 receives voltage from shunt, through R20 and R18. When no load is connected at output, negative 0V reach pin-2 of IC1 and positive 0V reach pin-3. This results in high output at output pin-1 of IC1. High output at pin-1, turns on the Light Emitting Diode D10 connected to that pin. This indicates that inverter is on, but no load is connected at its output.

High output at pin-1 is given to pin-10 of IC1 through R3 and D5. Capacitor C1 at pin-10 will slowly increase the voltage at this pin. Pin-9 of IC1 receives +5V regulated supply from an external source. As C1 charges, voltage at pin-10 increases; when the voltage at pin-10 becomes higher than the voltage at pin-9, a high voltage (10V) is output from output pin-8. This high output is given to the base of T3, through R34, D11 and D10.

High voltage at the base of T3, switch on the transistor and a 0V is output from its collector. This 0V reach the pin-1 and 5 of another IC2 called NAND gate (CD4011), IC2 is a Quad 2 input NAND gate. Pin-1 and 5 are input pins of two of the NAND gates inside the IC package. When pin-1 and 5 receive 0V, output pins 10 and 11 of the NAND gate will stop the output of MOS drive voltage. With the absence of the MOS drive signal from IC2, the MOSFETs in the output section will stop functioning. This will stop the output at the inverter

output socket, that is, the inverter shuts down. The shutdown circuit comprises of pin-8, 9 and 10 of Op-Amp (IC1), transistors T6, T9 and the circuit arrangement of IC2; this is shown in figure 3.

3.1.4 "No Load" Indication.

High voltage at pin-8 of IC1 is given through R8, to the following.

- LED D8, through R2
- Buzzer, through D1 and R1

This will switch on the LED D8 and buzzer will sound, indicating no-load condition.

3.1.5 Attaching load when Inverter is in "No Load" condition.

During the no-load shutdown condition, when a load is connected to the inverter output socket, a positive 0V develops at the output section of MOSFETs source. This results in a positive 0V at pin-2 of IC1. When positive 0V reach pin-2 and 3 of IC1, 0V is output from its pin-1. This will stop the voltage at pin-10 from increasing and a continuous low voltage is produced from its output pin-8. This results finally in normal operation of the inverter.

3.2 Low Battery Shutdown Section

To protect the battery- a device that serves as input to the inverter system- and to ensure a longer life span of the battery, a low battery detector/shutdown circuit is used. When the battery discharge to a preset level, the low-battery shutdown section sounds the buzzer for some time and then automatically shuts down the inverter. When a 12V battery reaches 10V, it is considered completely discharged (Jung, 2004). Once the battery is discharged to 10V, it requires charging before it can be used. The inverter system therefore automatically shuts down itself when the battery voltage reaches 10V to protect the battery from getting damaged.

3.2.1 Low Battery Shutdown Circuit

Low battery shutdown circuit consists of Op-Amp made of pin-5, 6 and 7 of IC1. Pin-5 of IC1 receives +5V regulated supply as reference voltage from an external source. Pin-6 receives battery supply through the potential divider R16 and R17. Pin-7 is output pin.

3.2.2 Working Principle of Low Shutdown Circuit

When the battery has enough charge, the voltage at pin-6 is higher than the voltage at pin-5. For example, when the battery is fully charged (13.5V), pin-6 has around 8.7V, as the battery gets discharged to around 12V; the voltage at pin-6 reduces to about 7.2V. As the battery gets discharged, the voltage at pin-6 gets further reduced. When the voltage at pin-6 becomes a little higher than the voltage at pin-5, output pin-7 will output a high signal (around 8.5V).

High output at pin-7 of IC1 will reach the following through R7:

- Low battery indicator LED D9, through R4
- Positive terminal of buzzer through D2 and R1
- Pin-10 of ICI through R5, D3 and R9.

     High voltage at D9 and buzzer will turn on the LED and starts sounding the buzzer. This alerts the user about low-battery shutdown. Turning on of LED D9 and sounding of buzzer indicate that the battery has reached 10V level, but low-battery shutdown has not yet taken place. High voltage at pin-7 of IC1 reaches pin-10 of IC1, through R5, D3 and R9. This repeats the whole process of inverter shutdown which was explained in the no-load shutdown section. Voltages at the various pins were measured, recorded and tabulated under different conditions of the battery level. Table 1 shows the voltage at various pin points of IC1 before the low-battery shutdown occurs.

     It should be noted that pin-6 of IC1 receives 8.7V only when the inverter battery is fully charged, that is the battery voltage will indicate around 13.5V. As the battery voltage reduces, the voltage at pin-6 also gets reduced. Table 2 shows the voltages when the low-battery starts sounding while table 3 shows the voltages after the low-battery shutdown occurs.

3.3 Overload Shutdown Section

If a load higher than the inverter capacity is connected at the inverter output, the MOSFETs at the output, and the output mains transformer could get damaged (Manahar, 2004). To protect the inverter from this situation, an overload shutdown section is used in the inverter. This section protects the inverter mains transformer and MOSFETs by switching off the inverter output. When the overload occur, the inverter does not switch off immediately; it indicates this condition by lighting an overload Light Emitting Diode (LED) and sounding buzzer before shutting down the inverter.

3.3.1 Overload Circuit

Overload shutdown section uses two Op-Amps using Pin-12, 13, 14, and 8, 9, 10 of IC1, transistors T4 and T3.

3.3.2 Working Principle

Load sensing voltage is given to the pin-12 of IC1 from source of MOSFETs, through R20, R18. Pin-13 of IC1 receives a constant reference voltage, through R14, R15 and overload adjustment preset VR1. The value of

reference voltage at pin-13 of IC1 is around 0.05V; this value can be increased / decreased by VR1. According to Phillip et al, 2002, a 500VA/12V inverter should be set for overload cut at 300W. When a 300W load is connected to the inverter, pin-12 of IC1 receives around 0.03V from the MOSFETs source. When more than 300W load is connected to the inverter, this results in 0.04V at pin-12 of IC1.

When the load is further increased, a point is reached when the voltage at pin-12 of IC1 becomes a little higher than the voltage at pin-13. This results in a high output (around 5.5V) at pin-14 of IC1. High output at pin-14 is given to pin-10 of IC1 as input, through R10 and D7. A high voltage at pin-10 results in high voltage (around 8V) from the output pin-8 of IC1. High voltage at pin-8 of IC1 repeats the whole process of inverter shutdown which was explained in the no-load shutdown section.

4. CONCLUSION

The use of an Op-Amp to provide safety for electronic device is very vital as it ensures the longevity of the electronic systems. The incorporation of Op-Amp inside an inverter system has a lot of advantages over the ones that does not have the Op-Amp feature. The Op-Amp design discussed in this paper does not only ensure the safety of the inverter system; it also ensures that all the peripherals, battery for example, used with the inverter system are protected from damage that could result from overuse.

REFERENCES

Horowitz, P. and Hill, W. 1989. The Art of Electronics. Cambridge University Press, Cambridge, pp. 176-180, 284-285.

Jung, W.G. 2004. OP Amp Applications Handbook. Newness, pp. 777-779.

Stout, D.F. 1976. Handbook of Operational Amplifier Circuit Design. Mc Graw-Hill, pp.1-11.

Malmstadt, E. 1981. Electronics and Instrumentation for Scientists. The Benjamin/Cummings Publishing Company Inc., pp.108–110.

Manahar, L. 2004. Modern Uninterrupted Power Supply – Introduction, Servicing and Troubleshooting. B.P.B publication, New Delhi, India. pp. 23-48.

Phillip, A. and Douglas, H. 2002. *CMOS Analog Circuit Design*, Oxford University Press, Oxford, pp.55-58.

Rogenmoser, R. and Kaeslin, H. 1997. The impact of transistor sizing on power efficiency in submicron CMOS circuits. Solid-State Circuits, IEEE Journal 32 (7), pp. 1142–1145.

Table1: Voltage at various points before Low-battery shutdown.

PIN	VOLTAGE
5	5.0V
6	8.7V
7	0V
8	0V
9	5.0V
10	0V

Table2: Voltages when the Low-Battery Buzzer starts sounding.

PIN	VOLTAGE
5	5.0V
6	4.0V
7	8.5V
8	0V
9	5.0V
10	0V

Table 3: Voltages after the Low-Battery Shutdown

| PIN	VOLTAGE
5	5.0V
6	4.8V
7	8.5V
8	10.5V
9	5.0V
10	5.1V
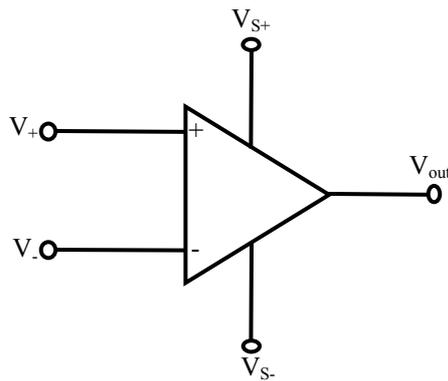
Figure 1. Circuit diagram/symbol for an Op-Amp.
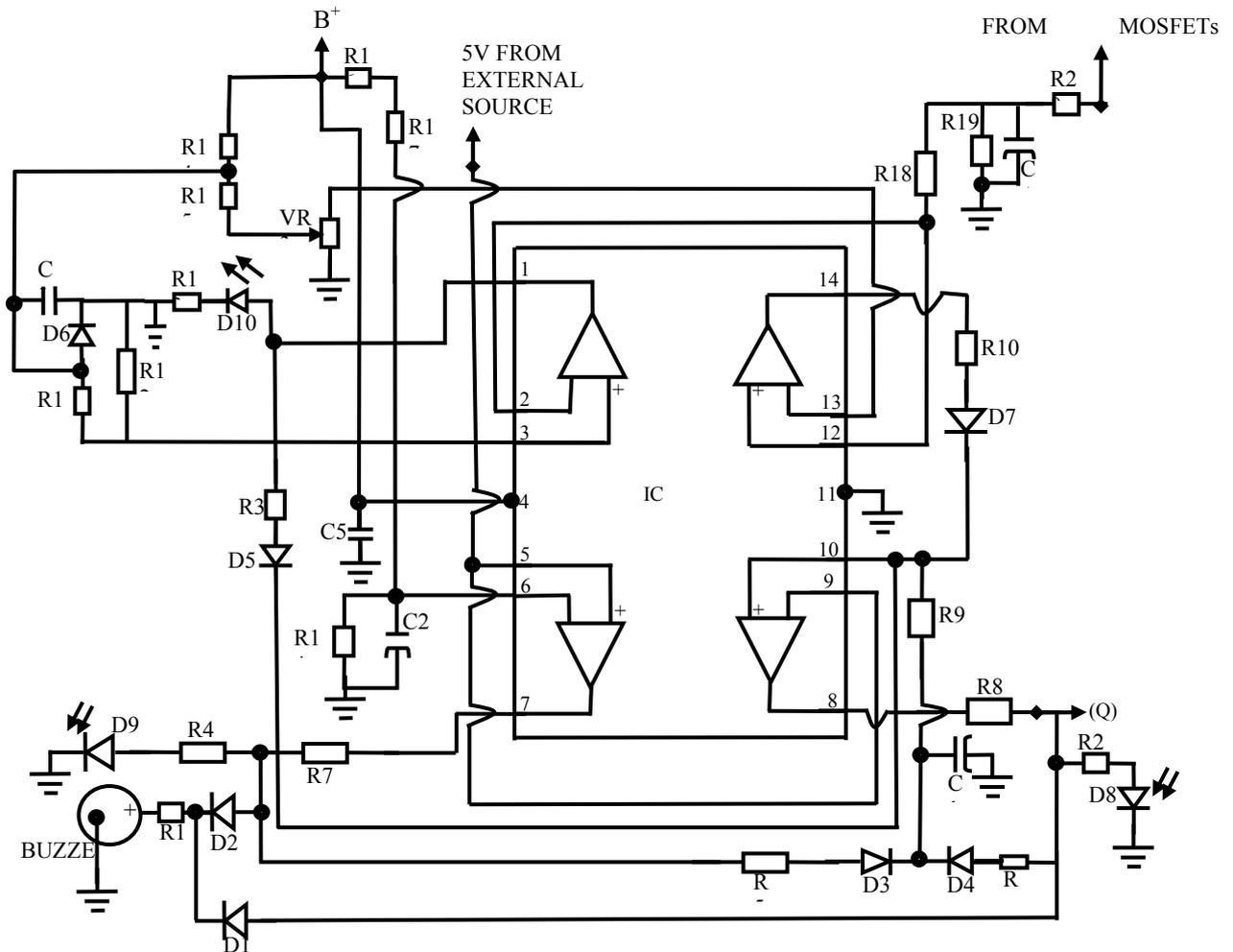
R1=R2=R4=R10=R13=R20=2.2K,   R19=100K,   R7=R8=R9=R18=1Ω,
R6=R11=R14=R17=47K, R5=330K, R16=4.7K, R15=22K, R3=1M, R12=47 Ω
D1=D2=D3=D4=D5=D6=D7=IN4148,   D8=OVERLOAD/SHUTDOWN
LIGHT EMITTING DIODE (LED) INDICATOR, D9=LOW BATTERY LED
INDICATOR, D10=NO-LOAD LED INDICATOR, C1=47µF 50V, C2=10µF
50V, C3=0.22µF 100V,C4=100µF 50V, C5=0.1µF 100V, IC1=LM324 (QUAD
OPERATIONAL   AMPLIFIER) ,   VR3   (OVERLOAD   ADJUSTMENT
PRESET) =4.7K, B+=REGULATED 12V SUPPLY FROM BATTER.

FIGURE 2: PROTECTIVE CIRCUIT USING OP-AMP
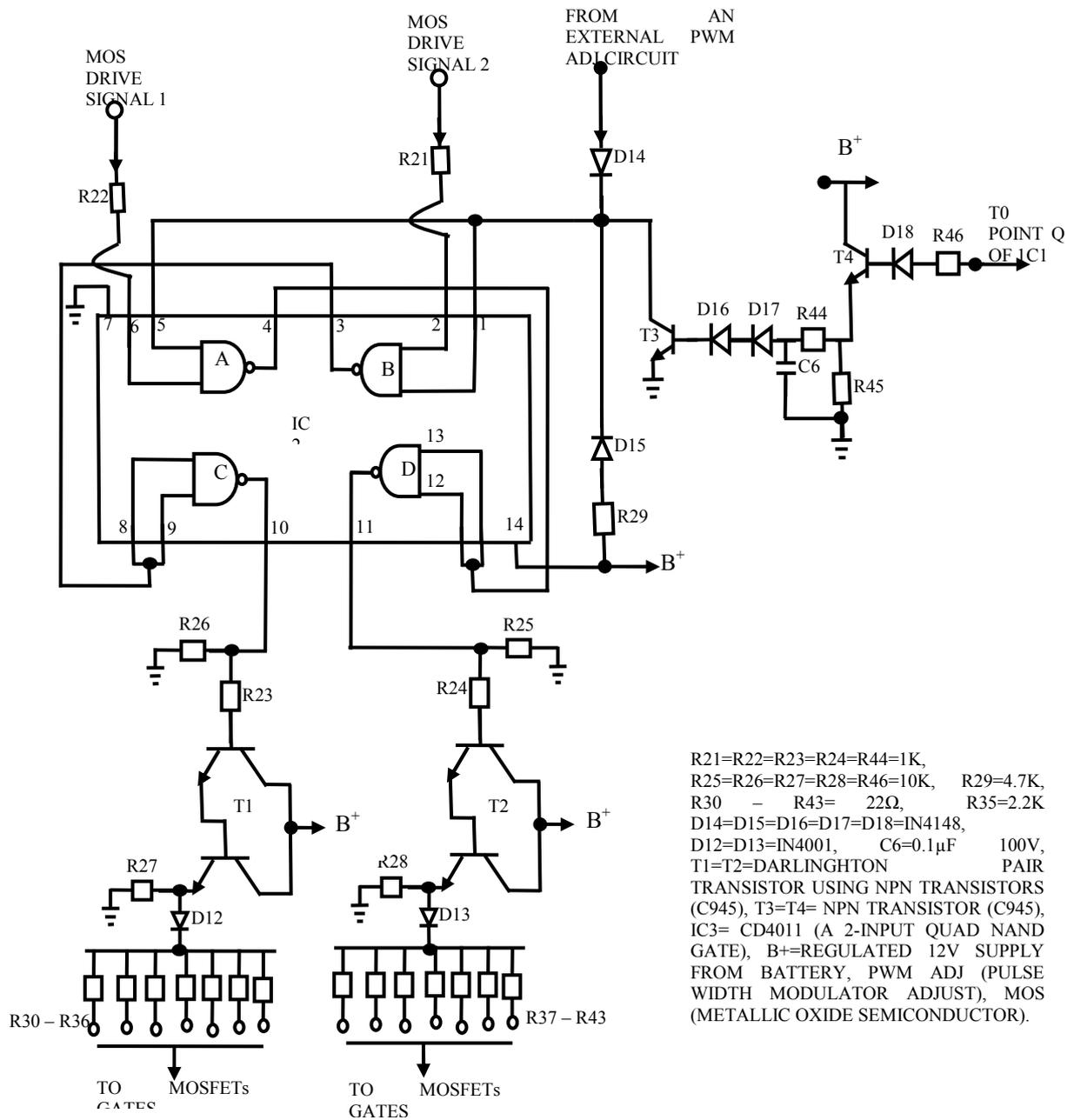
FIGURE 3: SHUTDOWN CIRCUITRY USING NAND GATE AND MOS DRIVER SECTION

R21=R22=R23=R24=R44=1K, R25=R26=R27=R28=R46=10K, R29=4.7K, R30 – R43= 22Ω, R35=2.2K D14=D15=D16=D17=D18=IN4148, D12=D13=IN4001, C6=0.1μF 100V, T1=T2=DARLINGHTON PAIR TRANSISTOR USING NPN TRANSISTORS (C945), T3=T4= NPN TRANSISTOR (C945), IC3= CD4011 (A 2-INPUT QUAD NAND GATE), B+=REGULATED 12V SUPPLY FROM BATTERY, PWM ADJ (PULSE WIDTH MODULATOR ADJUST), MOS (METALLIC OXIDE SEMICONDUCTOR).

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