Journal of Information Engineering and Applications
ISSN 2224-5782 (print) ISSN 2225-0506 (online)
Vol.5, No.8, 2015

Energy Optimization for Low Power Embedded Systems

Shariq Hussain
Department of Software Engineering, Rawalpindi Campus, Foundation University Islamabad, Pakistan

Abstract

The advancement in semiconductor technology enabled development of miniature handheld embedded systems running on battery source. The lifetime of battery plays an important role in the operation of these devices. In this work, a memory management technique is presented to optimize the energy consumption of embedded systems. The technique is applied on hardware level to optimize the energy consumption and to enhance the battery life of low power embedded systems. The analysis of results shows significant reduction in power consumption and improvement in battery lifetime.

Keywords: Embedded Systems, Memory Management, Energy Optimization, Battery Performance.

1. Introduction

Embedded systems are designed as combination of hardware platform and software layers to perform a dedicated task often with real time computing constraints [1]. Whereas a general purpose computer is more flexible and can perform wide range of operations. Embedded systems are controlled by one or more processing units or Digital Signal Processors (DSPs).

Over the past few years the range of applications using embedded systems has dramatically increased with wider deployment of computers. This increase means more energy consumption for these systems. In this work, a scheme is proposed to reduce the power consumption in Smart-Badge [2] a wearable system based on the ARM microprocessor developed by HP Labs without compromising flexibility, functionality, and performance of the system.

The method employed for power optimization is applied only to memory organization as power and performance of the system is heavily effected by memory organization for a given memory access pattern. Keeping the system memory in live state all the time consumes more power which can ultimately reduce battery life. By lowering the power supply or shutting down parts of memory that are not in use, power consumption can be reduced. The solution is implemented at hardware level for Smart-Badge. Switching off the unused parts of memories is an effective way to reduce power that ultimately reduces power consumption which can be attributed to longer battery life.

This paper is organized as follows: Section 2 presents related some and system model is described in Section 3. Section 4 discusses the methodology adopted for this work. Experimental results are presented in Section 5 and Section 6 concludes the paper.

2. Related Work

Several techniques for software optimizations have been presented in the literature. These techniques rely on compiler-based optimizations for energy saving. Levy et al. [3] state that the memory of a system contributes more than 50% in power consumption in battery operated embedded systems. The focus is given to compiler-based memory management techniques to conserve energy of the system. Grun et al. [4] implemented a profiling technique based upon the memory access patterns. Several techniques for power optimization specific to the processing elements (PEs) are discussed and some code optimization by reducing the memory accesses [5]. Scheduling techniques can also be applied for memory savings, and minimizing device state transitions [6]. In this work, the proposed scheme reduces the power consumption of the embedded system by partitioning memories into smaller blocks and switching off the unused portions of memory, resulting longer battery life.

3. System Model

The system under consideration is a modified version of Smart-Badge [2] as shown in Figure 1. The system consists of ARM processor, two level of cache i.e. L1 & L2, RAM, flash memory, Datapath Control and buffer, Memory Control and buffer, DC-DC converter and battery.

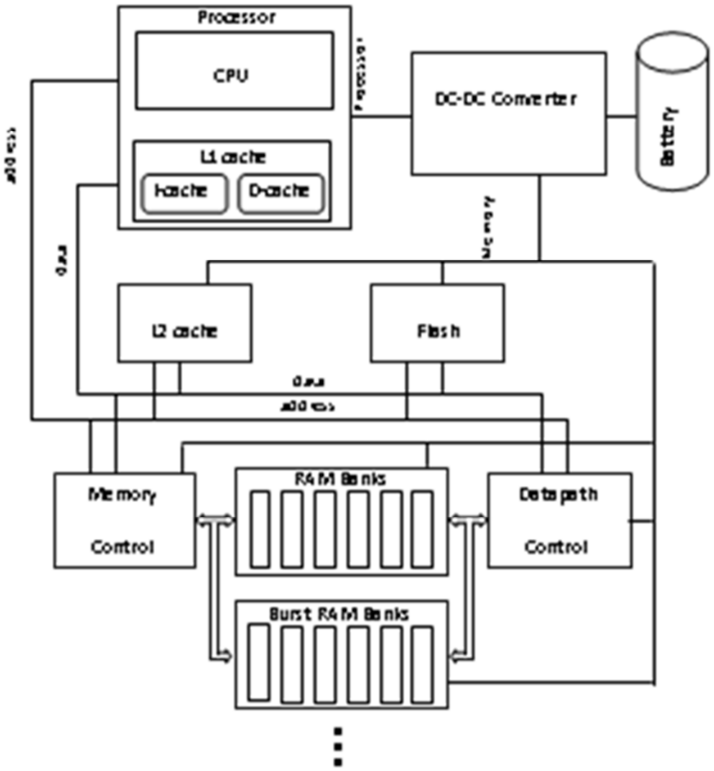

Figure 1. System model

4. Methodology

Memory is an important part of every computing system that is required to perform computational tasks. During the early stages of computing technology, the memory was expensive and had limited space due to high manufacturing costs. Therefore the focus was on memory size optimization techniques to use the available memory in best possible way. With the advancement of integrated circuit technology, now more transistors can be integrated into smaller chips and cost of memory is extremely low. In battery-operated systems, memory performance and power consumption is now a major challenge in the system design. The easiest memory model is flat memory model, assuming that data is stored in a single large consecutive memory space. With the increase of memory size, access to address space become slower and require more power.

In order to minimize the power consumption, memory is subdivided into number of smaller separate blocks or memory banks. This division helps in reduction of memory latency timing in a certain level. To implement this scheme, one datapath control with buffer and one memory control with buffer added to the embedded system. The function of memory control/buffer is to route the memory access to the RAM by providing row/column address strobes, addresses, and controls sequencing. The datapath control/buffer provides non-blocking external memory access, and generates an interrupt to the CPU when the data from RAM is available.

The main idea for memory partitioning is to divide the one single large memory address space into smaller blocks that can be switched on and off independently to conserve energy. Power consumption for memory access is decreased when the number of memory banks are small. However, an overly formation of large number of small banks imposes drawbacks, i.e., increase in wiring overhead complexity and highly area inefficient, thus tends to draw more power for communication. Due to this reason, formation of memory banks is subject to above mentioned constraints.

In order to calculate the energy consumption, let's assume that the memory address space is within the range from *0* to *M-1*. The dynamic access of target application is defined in the form of two arrays, i.e., **rd** = [rd_0, rd_1, …, rd_{M-1}], **wr** = [wr_0, wr_1, …, wr_{M-1}] where rd_i denotes the number of read requests to address *i*, and wr_i is the number of write requests to the address *i*. We can define *hi* and *low* as maximum and minimum address in range. The total energy consumption by memory, holding a given address space, can be calculated by a function:

$$MemE\ (low, hi, \mathbf{wr}, \mathbf{rd}) = E_{rd}(hi - low) \cdot \Sigma\, rd[i] + E_{wr}(hi - low) \cdot \Sigma\, wr[i] + E_{bank}\ (n)$$

The above function is a monotonous in nature as it increases with the increase in memory size i.e. (*hi – low*). *MemE* is the resultant of product of two functions of memory size, i.e., first is the energy for the read/write requests and the second is sum of read/write requests count.

5. Experimental Results

In order to test the system, simulator was used with 256K memory in the system. Memory was partitioned into 8 banks of size 4K each. Each bank consumes .1 energy and for 8 banks consumption it becomes .8 i.e. for full flat memory access. Energy for Er is 0.03 and for Ew is 0.05. Four different applications were executed on the system. All applications performed some read/write operations with different memory requirements. Tests were conducted with flat memory model and then with partitioned memory model. Table 1 shows the simulation results for the Smart-Badge system.

Table 1. Simulation results

Application	Program Size	Energy		
		Flat	Partitioned	Savings
ABC	4K	1.55	1.3	8.06%
K2	7K	2.3	2.09	4.57%
MK	10K	1.8	1.57	6.39%
Z7	2K	1.67	1.38	8.68%

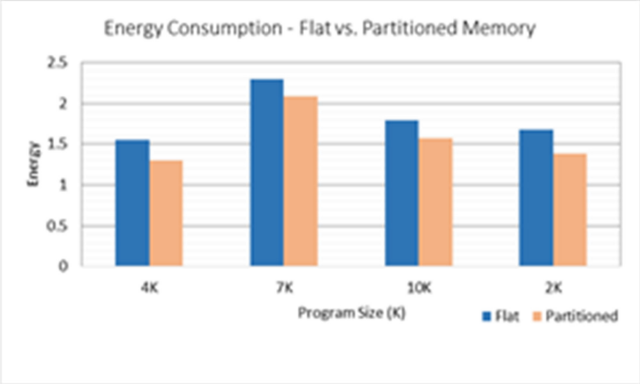

Figure 2. Energy usage – partition vs. flat

The results depicted in Figure 2 show a very clear picture and the energy savings are much larger as compared to flat memory usage. Another aspect is that the power consumption depends upon program size and read/write operations.

5. Conclusion

Flat memory scheme used in the embedded system is not power efficient and consumes more power as the whole memory is turned on during the operation of system. On the other hand a memory partitioning scheme is presented in which memory is partitioned into smaller banks. During the operation of system, unused banks are turned off to save the energy. Results showed energy savings up to 9%. Another area of interest for future work is to find an optimal memory partition size.

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