Journal of Information Engineering and Applications
ISSN 2224-5782 (print) ISSN 2225-0506 (online)
Vol.7, No.6, 2017

Asymmetric Cascaded Multilevel Inverter with Unequal Dc Sources using SPWM and MSVPWM Topologies

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Abstract
This paper introduces the modeling design and simulation of seven and thirteen levels cascaded asymmetric multilevel inverter (MLI) with reduced number of switches. MLI is the most efficient energy converters which are essentially appropriated for high power applications with decrease total harmonics distortion (THD). MLI doesn't only get high power in the output but it is also utilized in renewable energy resources such as fuel cells, wind and photovoltaic cells. This paper principally focuses on a hybrid cascaded MLI with two and three unequal dc supplies which decreases the number of semiconductor power switches. Sinusoidal PWM (SPWM) and modified space vector PWM (MSVPWM) techniques are used to improve an ac output with reduced THD. The gating pulses for seven and thirteen level hybrid cascaded converter using SPWM and MSVPWM techniques are introduced. The results of these proposed modulation strategies reduce the percentage magnitude of THD. The performance of the proposed SPWM and MSVPWM topologies are verified using seven and thirteen levels cascaded asymmetric MLI via simulink/matlab.
Keywords: Sinusoidal Pulse Width Modulation (SPWM), Modified Space Vector Pulse Width Modulation (MSVPWM), Multilevel Inverter (MLI), Total Harmonics Distortion (THD)

1. Introduction

The request for medium and high voltage, high power converters are increasing. It can't be connected directly with power switch to obtain high voltage grid. Therefore, the multilevel converters had been presented. The multilevel inverters are growing now. There are various types of array for dc voltage supplies, semiconductor power switches and diodes to produce a desired ac voltage output of multilevel inverters. When the number of levels is increasing, the staircase output waveform becomes like sinusoidal signal. The THD of output voltage is reduced. In addition it reduces switching losses, better electromagnetic interference (EMI), lower voltage stress of dv/dt on power switch and high efficiency [1-4]. These types of multilevel converters are divided into three major classifications flying capacitor, neutral point clamped and cascaded multilevel inverter [5-8]. The cascaded multilevel converter doesn't demand flying capacitors or diodes clamped. Moreover, these converters are reliable, simple to control and with reduced number of switches [9, 10]. As a result, the total cost and losses of these converters decreased and the efficiency is increased. Therefore, the cascaded multilevel converters became more important. These inverters are consisting of various arrays of semiconductor power switches and dc voltage supplies. Generally, these cascaded converters divided into principal combinations, symmetric cascaded MLI with equal value of dc voltage supplies and asymmetric cascaded MLI with unequal magnitude of dc voltage supplies. The asymmetric cascaded converter contains reduced number of switches and dc voltage sources. This asymmetric generates higher number of level at the output in comparison with symmetric. The composition space and the total cost of an asymmetric cascaded is lower than symmetric cascaded converter [9]. Until now, various basic unit and different cascaded MLI inverters have been proposed in literatures. Different symmetric cascaded MLI have been introduced [11-13]. It is also proposed another strategy with two various algorithms as symmetric and asymmetric [14]. The major defects of symmetric cascaded MLI is the demand high number of semiconductor power switches, driver circuits and power diodes because of the equal value of dc voltage supplies. In order to raise the number of levels in the output, the various asymmetric cascaded converters have been introduced [9, 14, and 15]. In this paper a new basic units single phase cascaded MLI is proposed with unequal dc sources and minimum number of power switches. These units are connected in series. The positive output levels are generated from series of basic unit. The H-bridge is connected with the output terminals of series unit converter. Single phase hybrid cascaded MLI seven and thirteen levels using SPWM and MSVPWM techniques are simulated in matlab/simulink software.

Jaydeep Lakwal et al. [16] presented the modeling and simulated of fifteen level hybrid inverter for photo voltaic using different dc sources, it consist of power switches, diodes and various dc supplies, the THD of the output voltage is high .

K.Rachel et al. [17] focused on a seven level cascaded MLI using PD, POD and APOD carrier overlapping SPWM techniques. It is implemented using two H-bridge, and the THD of the ac output voltage is very high.

M.Latha et al. [18] concentrated on the performance of MLI using SVPWM strategy. It has high dc

component that caused destroy in transformer, inductive load and other components because of the heat trouble.

Neeraj Seth et al. [19] proposed three-phase asymmetric MLI with reduced number of power switches to improved harmonics performance. Three phase seven level hybrid MLI is simulated in simulink/matlab, a dc component is appeared in spectrum, and this dc component is due to asymmetric positive and negative sides. This is caused heat trouble in inductive load and other components.

Principle of operation of asymmetric cascaded MLI with unequal dc sources is introduced in section II. Sinusoidal PWM and modified Space vector PWM strategies used to control the output are presented in section III and section IV respectively. The simulation results are explained in section V. Conclusion is introduced in section VI.

2. Asymmetric cascaded MLI with unequal dc voltage supplies

In this study, a single phase hybrid cascaded MLI systems are proposed. The principle of operation of the proposed ways will be presented for seven and thirteen level converters. However, the installation can be easily suitable to any number of levels. The proposed new basic unit for a sub MLI is shown in fig. 1. It consists of dc voltage source with two semiconductor power switches S1 and S2. The output voltage magnitudes for cases of switches S1 and S2 is given in table I. it is apparent that both of power switches S1and S2 could not be ON simultaneously because it will cause a short circuit across terminals of dc voltage supply. From the table I it is cleared that two levels of output voltage can be achieved.

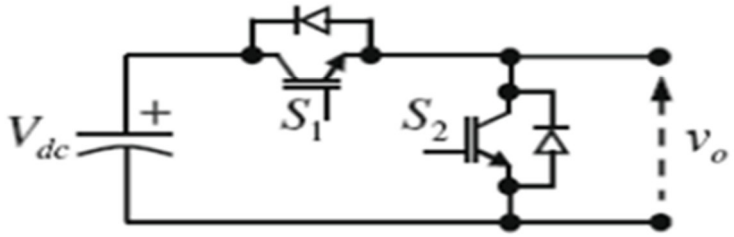


Fig. 1. The proposed new basic unit for a sub MLI [20]

TABLE I. The output voltage magnitudes for the two mode of operation

Mode	Switches cases		Output voltage
	S1	S2	
1	on	off	Vdc
2	off	on	0

Similarly, the output voltage signal for each basic unit can be produced in the same way. The different values of dc voltage supplies are connected to each basic unit. The output of cascaded basic units is connected to the full bridge drive. The output voltage of H-bridge (full-bridge) is appeared in positive and negative sides. The suggested asymmetric cascaded MLI is shown in fig. 2. The staircase ac voltage of proposed a hybrid cascaded MLI is similar to classical cascaded converter. The features of asymmetric MLI are simple structure, high efficiency, low cost and lower power switches losses. This asymmetric need lower number of power switches. The table II indicates the comparison between symmetric and asymmetric for a number of dc voltage supplies and semiconductor power switches.

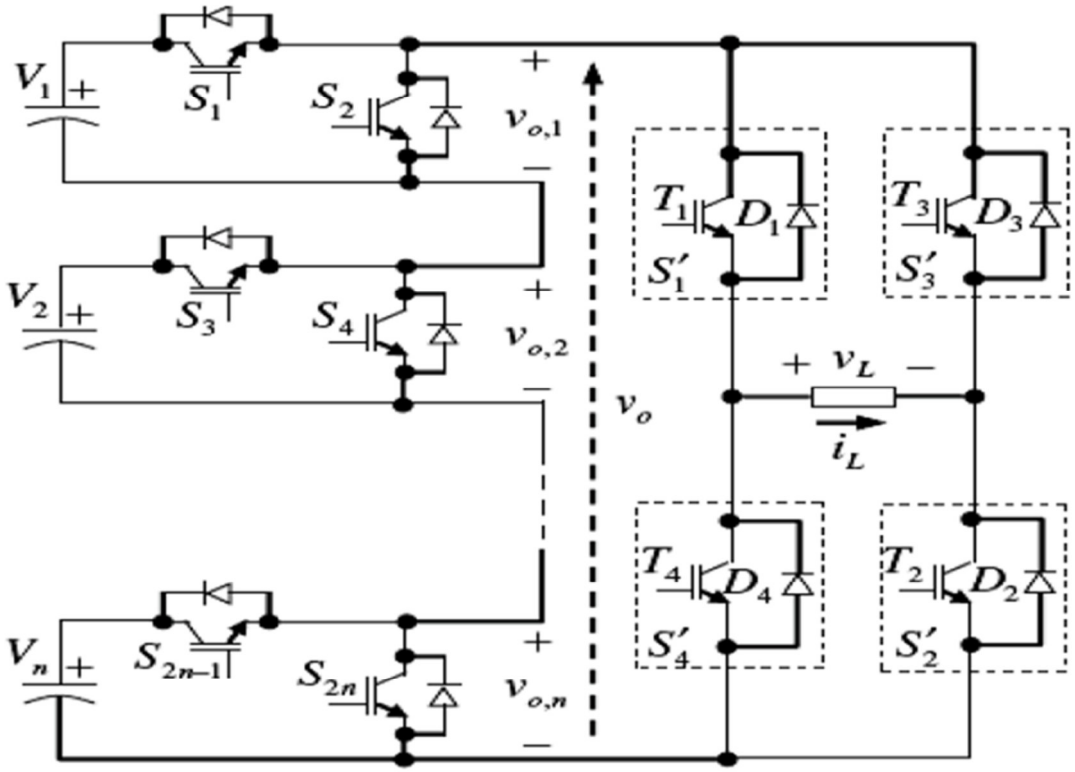


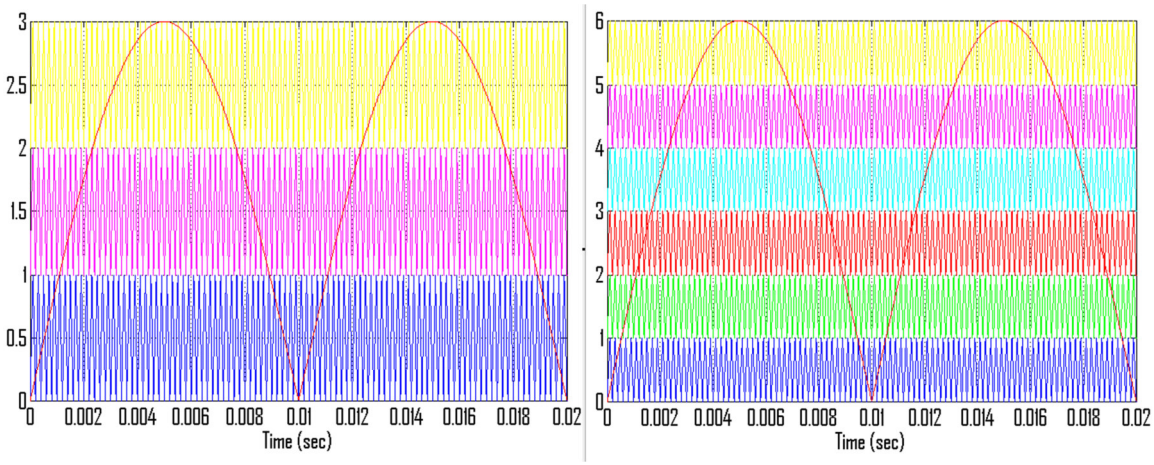
Fig. 2. The proposed hybrid cascaded MLI [20]

TABLE II. The Comparison between symmetric and asymmetric in term of number of switches for different number of dc voltage sources

Number of levels	Symmetric cascaded MLI		Asymmetric cascaded MLI	
	Number of dc supplies	Number of switches	Number of dc supplies	Number of switches
7	3	12	2	8
13	6	24	3	10

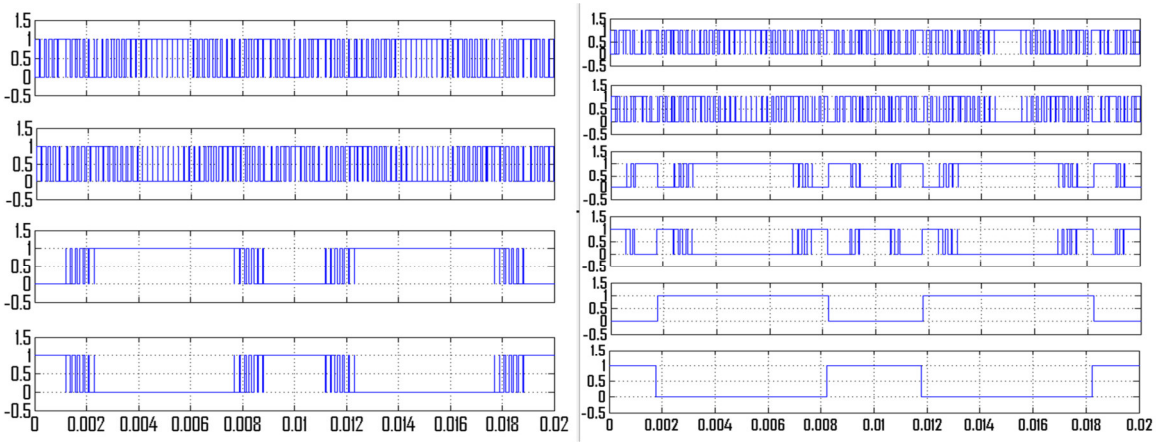
3. Sinusoidal PWM (SPWM) technique

To control the output signal in MLI, various modulation topologies have been utilized. Different pulse width modulation (PWM) techniques are applied for high switching in which the semiconductor power device is switched many time per half cycle [21]. In this study sinusoidal PWM technique has been used for control. The SPWM strategy is considered the most suitable control used via authors during in the literatures for MLI control. The principle of operation of SPWM topology is to produce the pulses by comparing sine reference modulation wave with a triangular carrier signal. The number of level is denoted as (n), the numbers of triangular carrier signals are (n-1). The saw tooth carrier signals has high frequency, this frequency called carrier frequency (fc), the peak amplitude of triangular signal is denoted as Ac. The frequency of the carrier wave determined the switching frequency of the MLI and the harmonics component of the output [22]. Furthermore, the sinusoidal modulation reference wave with peak amplitude Am has a low frequency (fm). The frequency of the sine wave determined the fundamental frequency in the output of the converter. The amplitude of sine wave controls the modulation index [23]. In case of MLI control, the sinusoidal reference modulation signal is compared with each triangular signal. This comparison is used to obtain the pulses that control semiconductor power switches. The semiconductor power device is turn ON when the sinusoidal signal is larger than the triangular wave linked with that semiconductor power switch. In this paper the reference sinusoidal wave is compared with six and twelve triangular signals as shown in fig. 3. The pulses of seven and thirteen level are generated by comparison and after a suitable logic circuit. A control pulse shown in fig. 4 is obtained.



(A) (B)

Fig. 3. The comparison between sinusoidal reference signal and triangular multicarrier signals (A) seven levels (B) thirteen levels

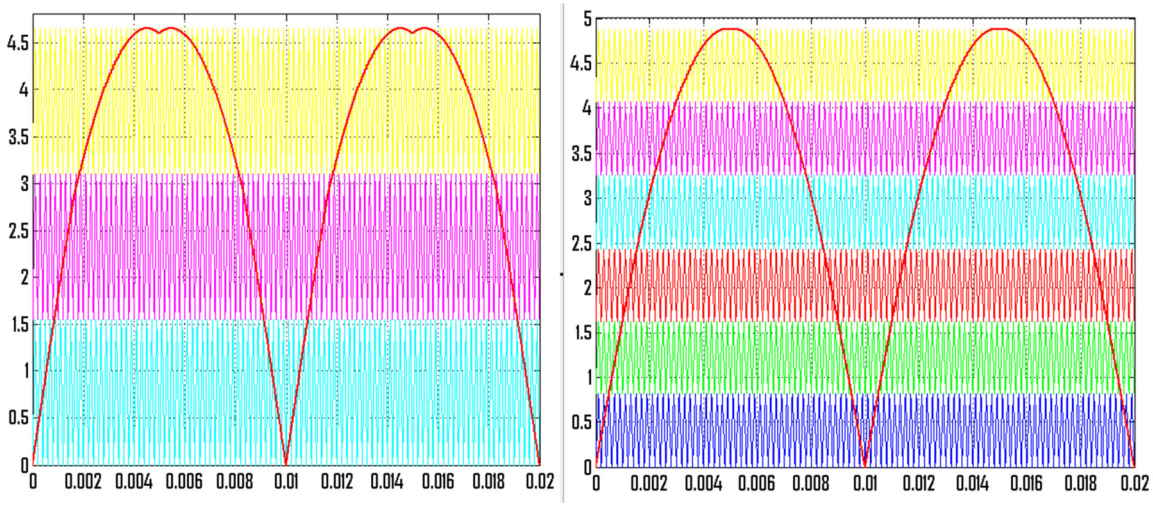


(A) (B)

Fig. 4. The pulses of SPWM asymmetric cascaded MLI (A) seven levels (B) thirteen levels

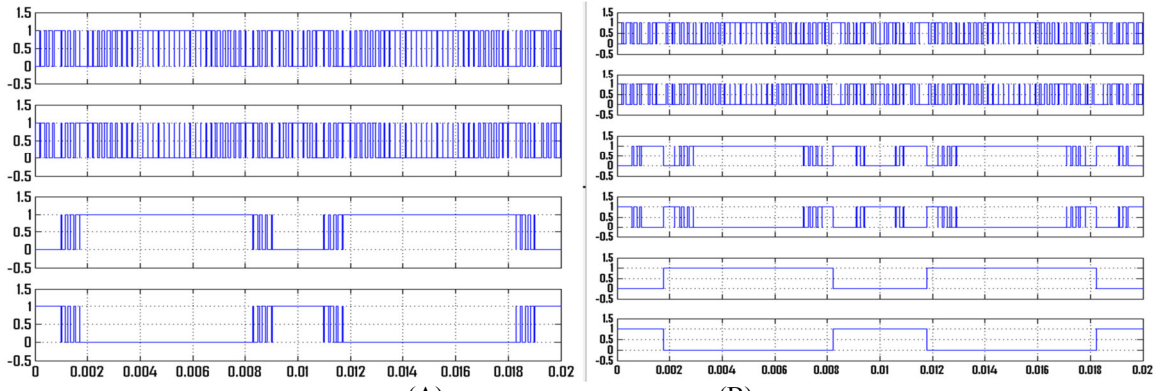
4. Modified Space Vector PWM (MSVPWM) technique

In the ordinary SVPWM for MLI involves mapping of the exterior sectors to an interior hexagon sector, to locate the switching time for various converter vector. It is apparent from the scheme in MLI will be very complicated because of the determination of switching times and sectors are increased. A modified scheme is presented in this work, where a fixed popular mode voltage is added to the supply phase voltage throughout the range of the modulation. The MSVPWM scheme topology has been presented, where the switching time for legs of MLI is directly identified from sampled amplitudes of phase voltage. This strategy reduces the calculation switches times more than classical SVPWM topology. This ordinary SVPWM works for a three level pulse width modulation (PWM) generation. It cannot be increased above three level inverters, because the determination of location becomes very complex. A saw tooth carrier based pwm strategy has been presented, where sinusoidal reference waves are added with appropriate offset voltage before the comparison with saw tooth carrier signals to realize the execution of a SVPWM [24]. The offset voltage determination is based on a coefficient function depending on voltage of dc link, the phase voltage amplitudes and number of levels in the output. The PWM switching time are applied for MLI legs. These PWM are immediately derived from the sampled amplitude of phase voltages, which is simple way for adding an offset voltage to the converter gating signal to produce the MSVPWM sample. The phase voltage with a desired offset voltage is compared with the triangular multicarrier signals as shown in fig. 5. The generated pulses of MSVPWM are shown in fig. 6. The proposed MSVPWM wave does not check for region limitation, sectors determination or look up schedules for switching vector identification, that it is needed in conventional multilevel MSVPWM topology. This proposed MSVPWM is efficient when it compared with ordinary multilevel SVPWM strategy.



(A) (B)

Fig. 5. The comparison between offset phase voltage signal and triangular multicarrier signals (A) seven levels (B) thirteen levels



(A) (B)

Fig. 6. The pulses of MSVPWM asymmetric cascaded MLI (A) seven levels (B) thirteen levels

5. The Simulation Results

The simulation results of the proposed MLI for seven and thirteen levels are presented using simulink/matlab program. The sinusoidal PWM and space vector PWM techniques are used to generate the control pulses. The frequency of sine reference wave and triangular carrier signal are 50Hz, 5KHz respectively. The IGBT semiconductor power switches are used. The IGBT has characteristic of fast switching capability. The load utilized in MLI is a resistive load. The output voltage includes seven and thirteen levels. The simulation matlab circuit for the proposed hybrid cascaded MLI of seven levels requires eight IGBT switches and two unequal dc sources as shown in fig. 7. The output voltage and FFT harmonics spectrum signals of SPWM and MSVPWM hybrid cascaded MLI for seven levels are referred in fig. 8 and fig. 9 respectively. The proposed asymmetric cascaded MLI requires ten IGBT switches and a third unequal dc sources for producing thirteen levels as shown in fig. 10. The ac output voltage and FFT harmonics spectrum of SPWM and MSVPWM hybrid cascaded MLI for thirteen levels are illustrated in fig. 11 and fig. 12 respectively. The staircase output voltage waveform has three levels in the positive side, three levels in negative side and a zero level, therefore there are seven levels. The staircase output voltage for thirteen levels has six levels in positive side, six levels in negative side and a zero level. Thus a hybrid MLI using SPWM and MSVPWM for seven and thirteen levels are successfully simulated.

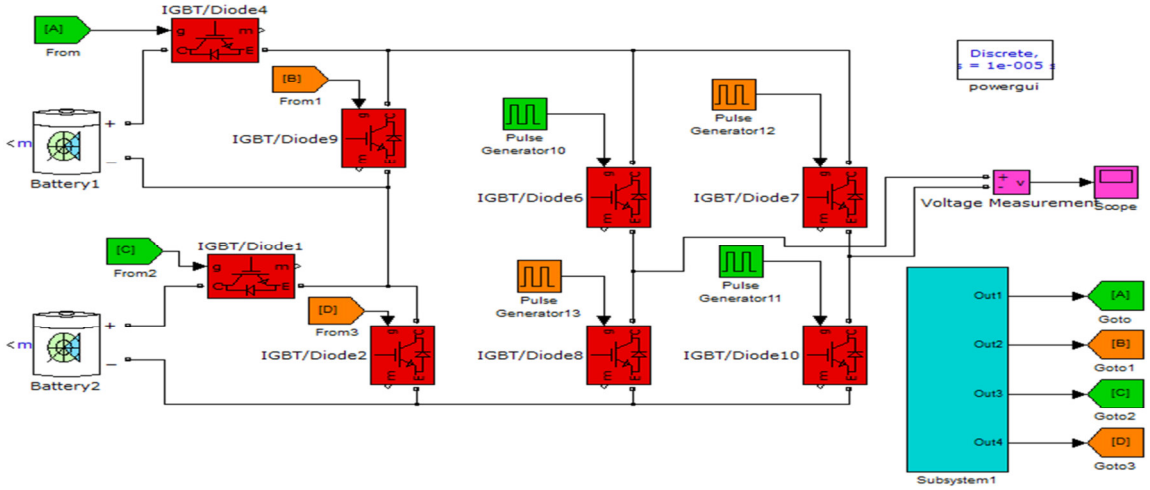


Fig. 7. The proposed asymmetric cascaded MLI of seven levels

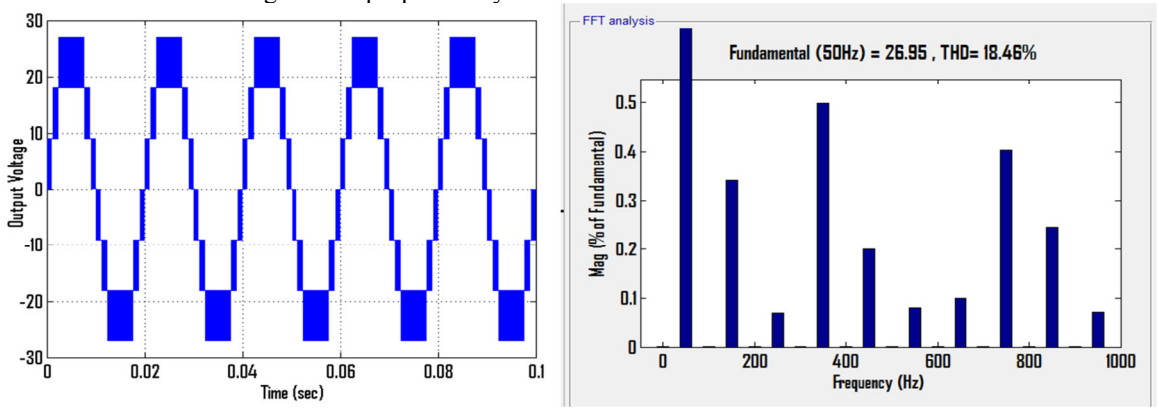


Fig. 8. SPWM technique hybrid cascaded MLI for seven levels (A) output voltage (B) FFT harmonics spectrum

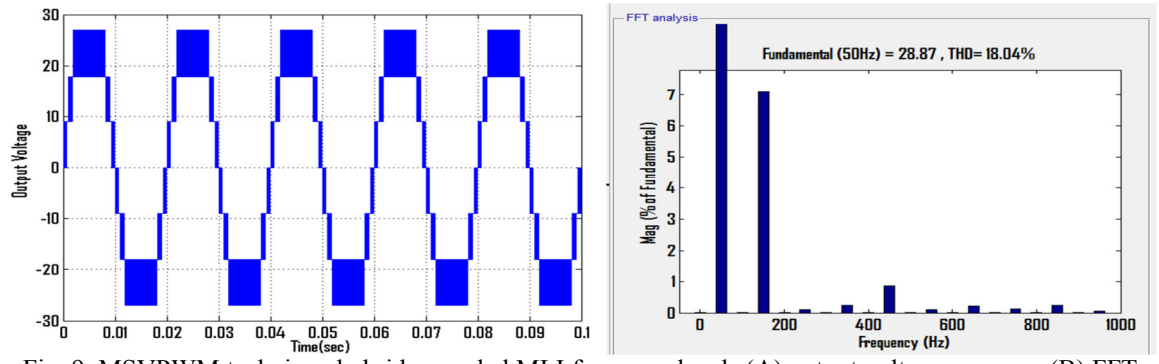


Fig. 9. MSVPWM technique hybrid cascaded MLI for seven levels (A) output voltage (B) FFT harmonics spectrum

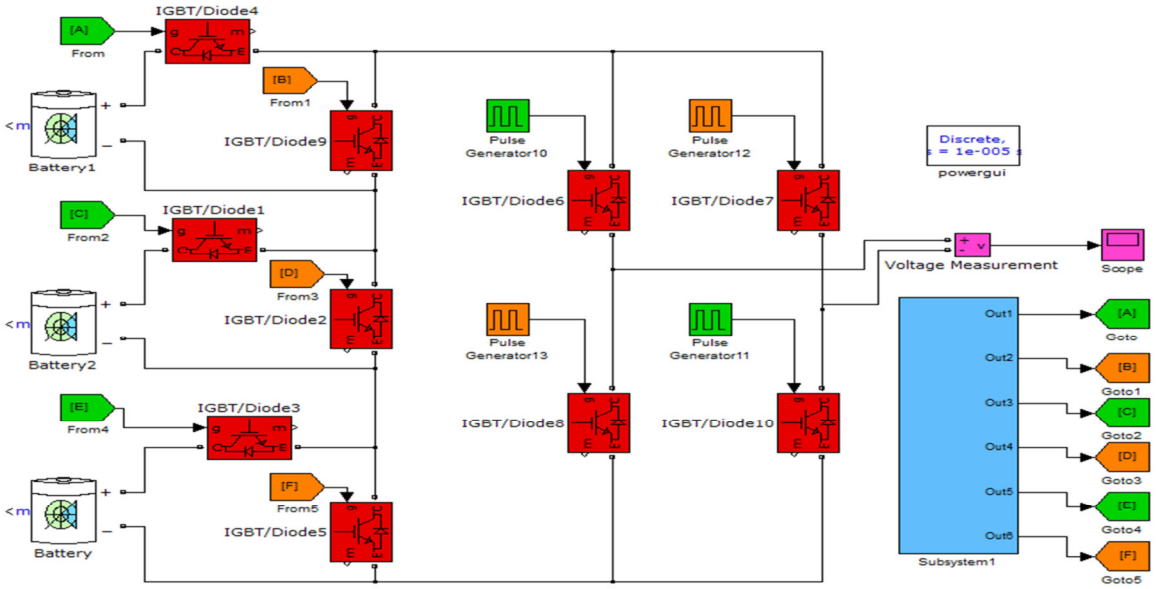


Fig. 10. The proposed asymmetric cascaded MLI of thirteen levels

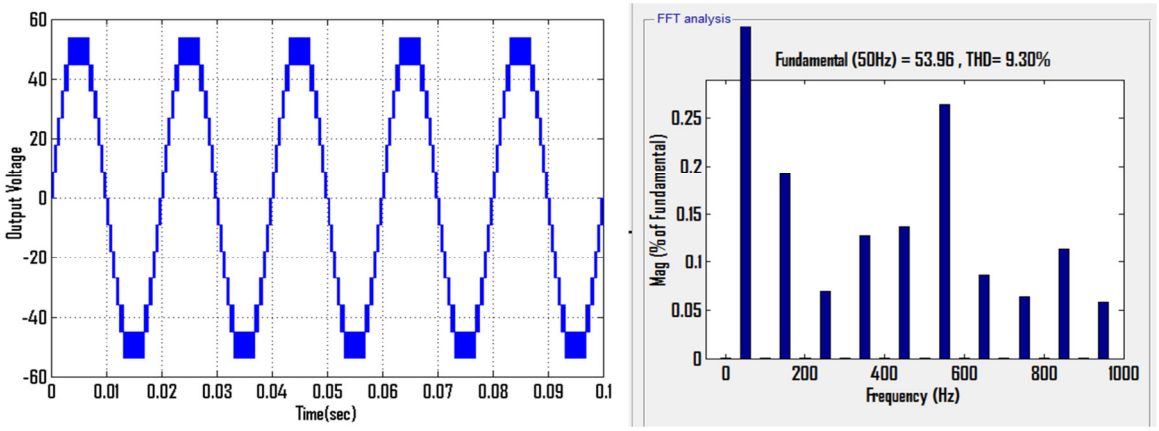


Fig. 11. SPWM technique hybrid cascaded MLI for thirteen levels (A) output voltage (B) FFT harmonics spectrum

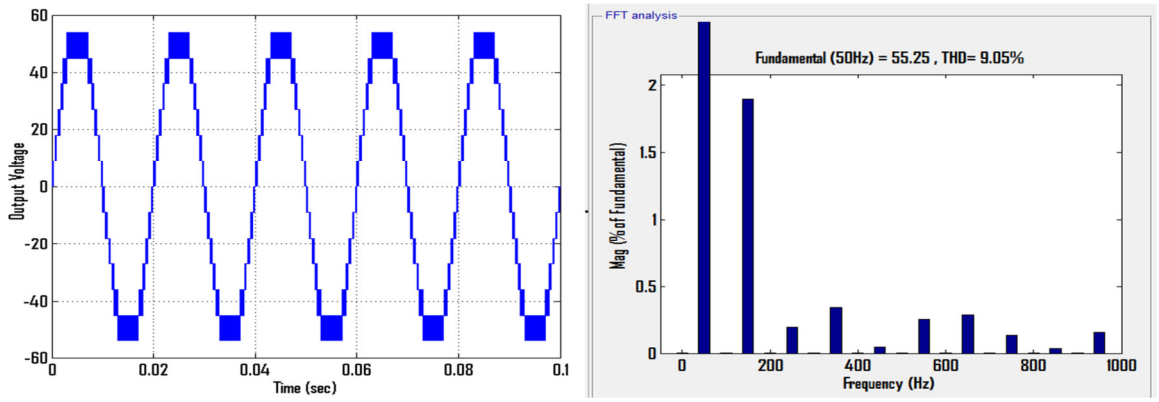


Fig. 12. MSVPWM technique hybrid cascaded MLI for seven levels (A) output voltage (B) FFT harmonics spectrum

TABLE III. The percentage value in term of THD between SPWM and MSVPWM

Number of levels	SPWM	MSVPWM
7	18.46%	18.04%
13	9.30%	9.05%

6. CONCLUSION

In this paper, a modern asymmetric cascaded MLI is presented. A single phase MLI structure for photovoltaic (PV) application using various dc voltage sources is proposed. The models and controls scheme of asymmetric MLI are introduced, simulation matlab illustrates the utility of the proposed systems. SPWM and MSVPWM techniques are used to control the switches. The percentage magnitudes in term of THD are compared as demonstrated in table III. The THD value of thirteen levels is lower than seven levels for both techniques SPWM and MSVPWM. In addition the MSVPWM strategy for seven and thirteen levels is lower than SPWM technique as it cleared in table III. The extension is easy of a hybrid cascaded MLI to get high number of levels in output. The suggested asymmetric cascaded MLI generates high levels of ac voltage signal. The staircase output voltage is approaching to sinusoidal signal by increasing the number of level. The hybrid cascaded MLI combination gives exactly appropriate results for producing the demand waveforms. The output voltage with low THD content could be acquired.

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