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Seven Level Modified Cascaded Inverter for Induction Motor Drive Applications

M.Murugesan
Faculty of Electrical and Electronics Engineering,
V.S.B Engineering College, Karur
Tamil Nadu, India
E-mail: murugesan.kec@gmail.com

S.Sivaranjani
Faculty of Electrical and Electronics Engineering,
V.S.B Engineering College, Karur
Tamil Nadu, India
E-mail: shivaranjani_s@rediffmail.com

G.Asokkumar
Faculty of Electrical and Electronics Engineering,
Annai Mathammal Sheela Engineering College, Namakkal
Tamil Nadu, India
E-mail: ganeshashokkumar@gmail.com

R.Sivakumar
Faculty of Electrical and Electronics Engineering,
V.S.B Engineering College, Karur
Tamil Nadu, India
E-mail: odaisiva@gmail.com

Abstract

In this paper, an H-bridge inverter topology with reduced switch count technique is introduced. This technique reduces the number of controlled switches used in conventional multilevel inverter. To establish a single phase system, the proposed multilevel inverter requires one H-bridge and a multi conversion cell. A multi conversion cell consists of three equal voltage sources with three controlled switches and three diodes. In conventional method, twelve controlled switches are used to obtain seven levels. Due to involvement of twelve switches the harmonics, switching losses, cost and total harmonic distortion are increased. This proposed topology also increases the level to seven with only seven controlled switches. It dramatically reduces the complexity of control circuit, cost, lower order harmonics and thus effectively reduces total harmonic distortion.

Keywords: Cascaded Multilevel Inverter, H-bridge Inverter, Total Harmonic Distortion, Sinusoidal Pulse Width Modulation, Insulated Gate Bipolar Transistor

1. Introduction

Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and MW power level. Therefore high power and medium voltage inverter has recently become a research focus. As far as conventional two level inverter is concerned, it exhibits many problems when used in high power applications (Franquelo 2008). Multilevel inverters have been gained more attention for high power application in recent years which can operate at high switching frequencies while producing lower order harmonic components. A multilevel inverter

not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind and fuel cells, which can be easily interfaced to a multilevel inverter system for high power applications (Rodriguez *et al.* 2002). There are several topologies such as diode clamped multilevel inverter or neutral point clamped inverter, flying capacitor based multilevel inverter, and cascaded multilevel inverter (Du *et al.* 2006). The main disadvantage still exists in diode clamped multilevel inverter topology, which restricts the use of it to the high power range of operation. Moreover flying capacitor based multilevel inverter also exhibits a disadvantage including more number of capacitors (Fang Zheng Peng 2001). The first topology introduced is the series H-bridge design, in which several configurations have been obtained. This topology consists of series power conversion cells which form cascaded H- bridge multilevel inverter and power levels will be scaled easily. An apparent disadvantage of this topology is large number of controlled switches. The proposed topology for multilevel inverter has seven levels associated with a seven number of power switches. In this proposed topology sinusoidal pulse width modulation technique is used.

2. Cascaded Multilevel Inverter (CMLI)

The general structure of cascaded multilevel inverter for a single phase system is shown in Figure 1. Each separate voltage source V_{dc1}, V_{dc2}, V_{dc3} is connected in cascade with other sources via a special H-bridge circuit associated with it. Each H-bridge circuit consists of four active switching elements that can make the output voltage either positive or negative polarity; or it can also be simply zero volts which depends on the switching condition of switches in the circuit. This multilevel inverter topology employs three voltage sources of equal magnitudes. It is fairly easy to generalize the number of distinct levels (Corzine *et al*. 2003 and 2004).

The S number of sources or stages and the associated number of output level can be written as follows

$$N_{level} = 2S + 1 \quad (1)$$

For example if S=3, the output wave form has seven levels ($\pm 3V_{dc}$, $\pm 2V_{dc}$, $\pm 1V_{dc}$ and 0). The voltage on each stage can be calculated by using the equation,

$$A_i = 1V_{dc}(i = 1, 2, 3 \dots) \quad (2)$$

The number of controlled switches used in this topology is expressed as,

$$N_{switch} = 4S \quad (3)$$

The output voltage of the multilevel inverter is given as,

$$V_o = A_1 + A_2 + A_3 \quad (4)$$

Where A_1, A2 and A_3 are DC voltage sources

The advantages of cascaded multilevel inverter are modularized layout and packaging. This enables the manufacturing process to be done more quickly and cheaply. The drawback of this topology needs a separate DC source for each of H-bridge and involves high number of semiconductor switches. Figure 2 shows the typical output voltage waveform of a seven level cascaded inverter with three separate DC sources.

3. Modified Cascaded Multilevel Inverter (MCMLI)

The general structure of a proposed cascaded multilevel inverter is shown in Figure 3. This inverter consists of a multi conversion cell and an H bridge. A multi conversion cell consists of three separate voltage sources (V_{dc1}, V_{dc2}, V_{dc3}), each source connected in cascade with other sources via a circuit consists of one active switching element and one diode that can make the output voltage source only in positive polarity with several levels. Only one H-bridge is connected with multi conversion cell to acquire both positive and negative polarity. By turning on controlled switches S1 (S2 and S3 turn off) the output voltage $+1V_{dc}$ (first level) is obtained. Similarly turning on of switches S1, S2 (S3 turn off) $+2V_{dc}$ (second level) output is produced across the load. Similarly $+3V_{dc}$ levels can be achieved by turning on S1, S2, S3 switches as shown in Table 1. The main advantage of proposed modified cascaded multilevel inverter is seven levels with only use of seven switches. The S number of DC sources or stages and the associated number output level can be calculated by using the equation as follows,

$$N_{level} = 2S + 1 \quad (5)$$

For an example, if S=3, the output wave form will have seven levels ($\pm 3V_{dc}$, $\pm 2V_{dc}$, $\pm 1V_{dc}$ and 0). Similarly voltage on each stage can be calculated by using the equation as given,

$$A_i = 1V_{dc}(i = 1, 2, 3 \dots) \quad (6)$$

The number switches used in this topology is given by the equation as follows,

$$N_{switch} = 2S + 4 \quad (7)$$

The switching table for modified cascaded multilevel inverter is shown in Table 1. It depicts that for each voltage level, only one of the switches is in ON condition among the paralleled switches. Multi conversion cell converts DC voltage into a stepped DC voltage, which is outputted as a stepped or approximately sinusoidal AC waveform by the H-bridge inverter. In this H-bridge, for positive half cycle, switches Q1 and Q2 will be turned on, similarly for negative half cycle switches Q3 and Q4 must be in ON condition. Figure 2 shows the typical output voltage waveform of a proposed cascaded multilevel inverter with three separate DC sources.

4. PWM for Harmonics Reduction

PWM technique is extensively used for eliminating harmful low-order harmonics in inverters. In PWM control, the inverter switches are turned ON and OFF several times during a half cycle and output voltage is controlled by varying the pulse width. SPWM techniques are characterized by constant amplitude pulses with different duty cycle for each period. The width of this pulses are modulated to obtain inverter output voltage control and to reduce its harmonic content. Sinusoidal pulse width modulation is the mostly used method in motor control and inverter application (Ismail 2006).In order to verify the ability of the proposed multilevel inverter topology to synthesize an output voltage with desired amplitude and better harmonic spectrum, programmed SPWM technique is applied to determine the required switching angles. It has been proved that in order to control the fundamental output voltage and eliminate 'n' harmonics, 'n+1' equations are needed. The method of elimination will be presented for 7-level inverter such that the solution for three angles is achieved. The Fourier series expansion of output voltage waveform using fundamental frequency switching scheme as follows

$$V_o(\omega t) = \sum_{n=1,3,5}^{\infty} \frac{4V_{dc}}{n\pi}(\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_K))\sin(n\omega t) \quad (8)$$

Where K is the number of switching angle required for 7 level inverter. Ideally, for a given fundamental voltage V_1, it is required to determine the switching angles $\theta_1, \theta_2, \ldots, \theta_K$ so that output voltage $V_o(\omega t)=V_1\sin(\omega t)$ and a specific higher harmonics of $V_n(n\omega t)$ are equal to zero. According to the three phase theory in balanced three phase system third order harmonic is cancelled. The switching angles can be found by solving the following equations

$$\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) = m$$
$$\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) = 0$$
$$\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) = 0 \quad (9)$$

Where modulation index, $m = \frac{V_1}{(\frac{4V_{dc}}{\pi})}$

One approach to solve the set of nonlinear transcendental equations (9), is to use an iterative method such as the Newton-Raphson method (Patel & Hoft 1973). In contrast to iterative methods, the approach here is based on solving polynomial equations using the theory of resultants which produces all possible solutions (Chiasson *et al.* 2003). The transcendental equations characterizing the harmonic content can be converted into polynomial equations. Then the resultant method is employed to find the solutions when they exist. These sets of solutions have to be examined for its corresponding total harmonic distortion (THD) in order to select the set which generate the lowest harmonic distortion (mostly due to the 11^{th} and 13^{th} harmonics). The computed THD in percent is defined by

$$THD\% = \frac{\sqrt{V_3^2+V_5^2+V_7^2+\cdots+V_{19}^2}}{V_1^2} \times 100 \quad (10)$$

Transforming the transcendental equations (9) into polynomial equations using the change of variables and the trigonometric identities

$$x_1 = \cos\theta_1, x_2 = \cos\theta_2, \ x_3 = \cos\theta_3, x_4 = \cos\theta_4,$$
$$x_5 = \cos\theta_5, \ x_6 = \cos\theta_6, \ x_7 = \cos\theta_7 \quad (11)$$

$$\cos(5\theta) = 5\cos\theta - 20\cos^3\theta + 16\cos^5\theta$$
$$\cos(7\theta) = -7\cos\theta + 56\cos^3\theta - 112\cos^5\theta + 64\cos^7\theta \quad (12)$$

To transfer (9) into the equivalent conditions

$$p_1(x) = x_1 + x_2 + x_3 + -m = 0$$
$$p_5(x) = \sum_{i=1}^{7}(5x_i - 20x_i^3 + 16x_i^5) = 0$$
$$p_7(x) = \sum_{i=1}^{7}(-7x_i + 56x_i^3 - 112x_i^5 + 64x_i^7) = 0 \quad (13)$$

System (12) is a set of three polynomial equations in three unknowns X_1, X_2, and X_3, where X=(X_1, X_2, X_3,) and the angles condition must satisfy $0 \leq X_1 \leq X_2 \leq X_3 \leq 1$. Polynomial systems are also considered to compute the solutions of the harmonic elimination equations by iterative numerical methods which give only one solution. In contrast, this system of polynomial equations will be solved using resultant such that all possible solution of (9) can be found. A systematic procedure to do this is known as elimination theory and uses the notion of resultants. The details of this procedure can be found in (Chiasson *et al.* 2004).

5. Simulation Result Analysis

The performance of the proposed modified cascaded multilevel inverter for induction motor drive is verified through the simulation results. It can be seen from Figure 3 input voltages for each succeeding voltage source is same. Figure 5 shows the simulation diagram of three phase modified cascaded multilevel inverter for induction motor drive. From that multilevel inverter seven level can be easily achieved by making the switching pulse sequences as shown in Figure 6a and Figure 6b. Figure 7a and 7b shows the output voltage waveform of single phase line to ground and line to line voltages of the proposed inverter. Figure 8a and 8b shows the output voltage waveform of three phase line to ground and line to line voltages of the proposed inverter. In this phase voltage is 220V and line voltage is 400V for seven level. Figure 9a and 9b shows the MATLAB simulation output waveform of speed and torque curve of induction motor. From the speed and torque curves, it is concreted that rated speed quickly achieved within 0.4 msec and the torque is quickly settled at 0.45 msec. Figure 10a shows the stator current waveform of induction motor. Therefore the proposed multilevel inverter can be used for variable speed drive application, which can be obtained by varying the frequency of multilevel inverter. From the FFT analysis it can be inferred that when the number of levels are increased, the harmonics and total harmonic distortion is reduced. Figure 10b shows THD value of proposed seven level inverter and it is 11.98%.

6. Comparison Results

Table 2 shows that the modified cascaded multilevel inverter involves only seven switches whereas conventional inverter comprises twelve switches, but in both cases input voltage at each stage and output level are same. Therefore the proposed modified cascaded multilevel inverter has less switching losses, simple control circuit and less complexity than conventional cascaded multilevel inverter.

7. Experimental Verification

Simulation of modified cascaded multilevel inverter output voltage is verified by single phase hardware prototype. Hardware prototype includes seven switches. Among those, three MOSFETs and three diodes are made available for a multi conversion cell. This cell consists of three power stages. In each power stage, one MOSFET (IRF250) and one diode are used as main switches, which are connected in modified configuration. Each stage is supplied by a symmetrical DC source. A PIC 16F877 microcontroller is used as the main processor, which provides gate logic signals. According to microcontroller control signal MOSFET gate terminal is turned on and off. Output of the inverter terminal is connected to R load. The hardware block diagram and prototype of modified cascaded multilevel inverter for a single leg are shown in Figure 11 and 12. Hardware result of proposed multilevel inverter is exposed in Figure 13. The resultant voltage of seven level

cascaded multilevel inverter is 9 volts, with frequency of 50 Hz.

8. Conclusion

This paper revealed that proposed modified multilevel inverter topology with reduced number of switches can be implemented for industrial drive applications. This multilevel inverter structure and its basic operations have been discussed elaborately. A detailed procedure for calculating required voltage level on each stage has been conversed. As conventional seven level inverter involves twelve switches, it increases switching losses, cost and circuit complexity The proposed inverter engages only seven switches with three diodes, which reduces switching losses, cost and circuit complexity. Moreover it effectively diminishes lower order harmonics. Therefore effective reduction of total harmonics distortion is achieved.

Appendix

Motor Details

Rotor Type: Wound

Power, Voltage and Frequency: 3730 W, 400 V and 50 Hz

Stator Resistance and Inductance: 1.115Ω and 0.005974Ω

Rotor Resistance and Inductance: 1.083Ω and 0.005947Ω

References

Franquelo, L.G., (2008), "The age of multilevel converters arrives", *IEEE Industrial Electronics Magazine*, Vol.2, No.2, 28-39.

Rodriguez, J., Lai, J.S. & Peng, F.Z., (2002) "Multilevel inverters: Survey of topologies, controls, and applications", *IEEE Trans. Ind .Appl*. Vol.49, No.4, 724-738.

Du, Z., Tolbert, L.M., Chiasson, J.N.& Opineci, B., (2006), "A cascaded multilevel inverter using a single dc power source", *Proc. IEEE APEC*, 426-430.

Fang Zheng Peng (2001), "A Generalized Multilevel Inverter Topology with Self Voltage Balancing", *IEEE Trans. Ind .Appl.* Vol.37, No.2.

Corzine, K.A., Wielebski, M.W., Peng, F.Z & Wang, J., (2004), "Control of cascaded multilevel inverters", *IEEE Trans. Power Electron*. Vol.19, No.3, 732-738.

Corzine, K.A., Hardick F.A, & Familiant, Y.L. (2003), "A cascaded multilevel inverter H-Bridge inverter utilizing capacitor voltage source", *Proceeding of the IASTED International Conference on Power and Energy Systems*, pp.290-295.

Ismail, B., (2006), "Development of a Single Phase SPWM Microcontroller-Based Inverter", *First International Power and Energy Conference PEC-IEEE*, 28-29.

Patel, H.S. & Hoft, R.G., (1973), "Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters: Part I – Harmonic Elimination", *IEEE Trans. Ind.Appl*., 3, pp. 310-317.

Chiasson, J.N., Tolbert, L.M., Mckenzie, K.J. & Du Z., (2003), "Control of a Multilevel Converter Using Resultant Theory", *IEEE Transactions Control System Theory*, Vol. 11, No.3, pp. 345-354.

Chiasson, J.N. Tobert, L.M., McKenzie, K.J. & Du, Z., (2004), "A Unified Approach to Solving the Harmonic Elimination Equations in Multilevel Converters", *IEEE Trans. Power Electron.*, Vol.19, No.2, pp. 478-490.

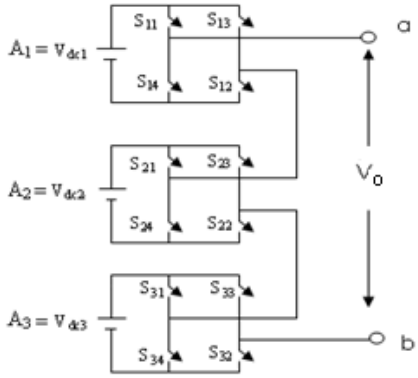


Figure 1. Topology for Cascaded Multilevel Inverter

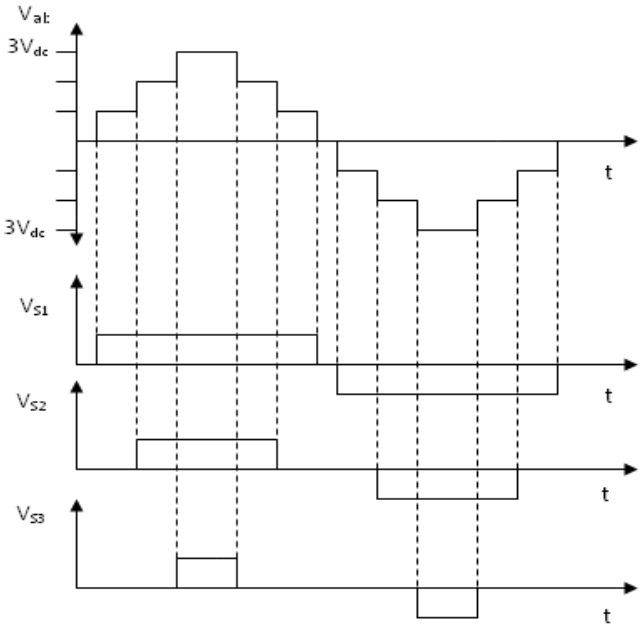


Figure 2. Typical Output Waveform for Cascaded Multilevel Inverter

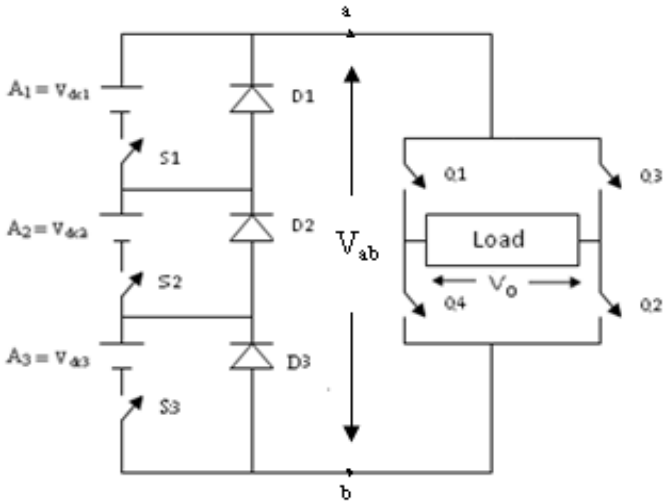


Figure 3. Topology for Modified Cascaded Multilevel Inverter

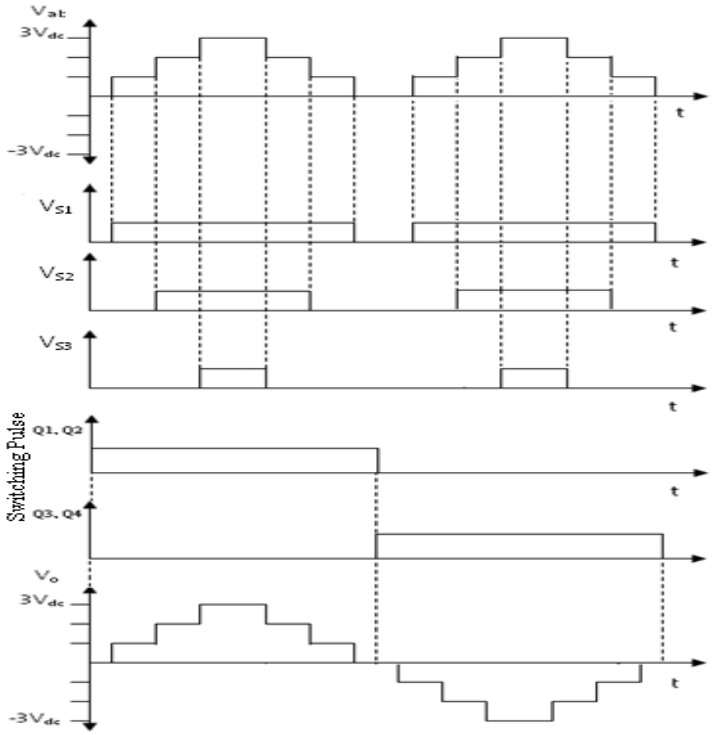


Figure 4. Typical Output Voltage Waveform of a Modified Cascaded Multilevel Inverter

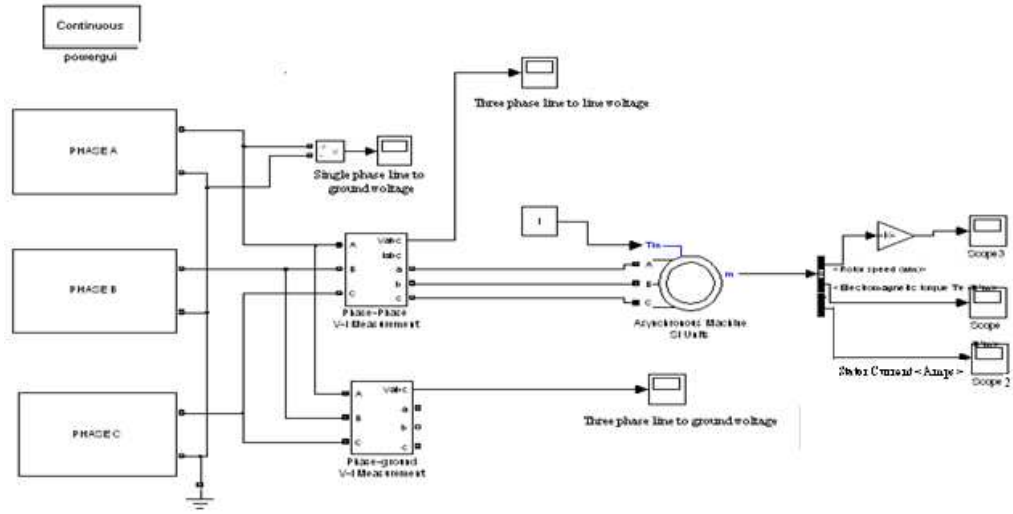
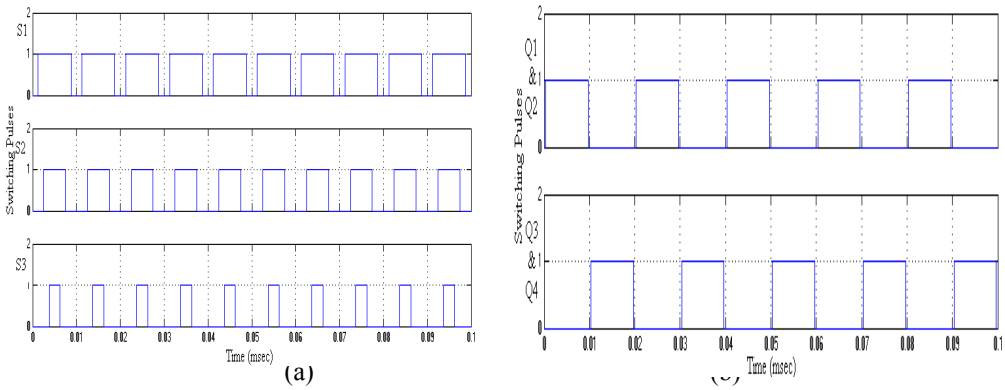
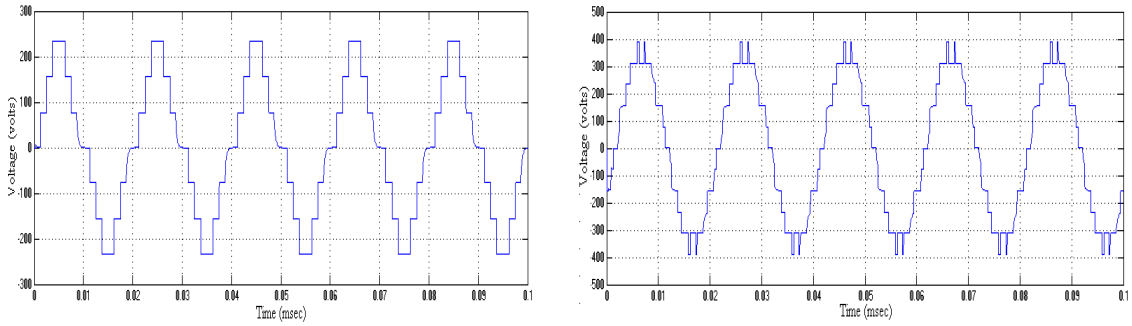


Figure 5. Simulation Diagram for Modified Cascaded Multilevel Inverter for Induction Motor Drive



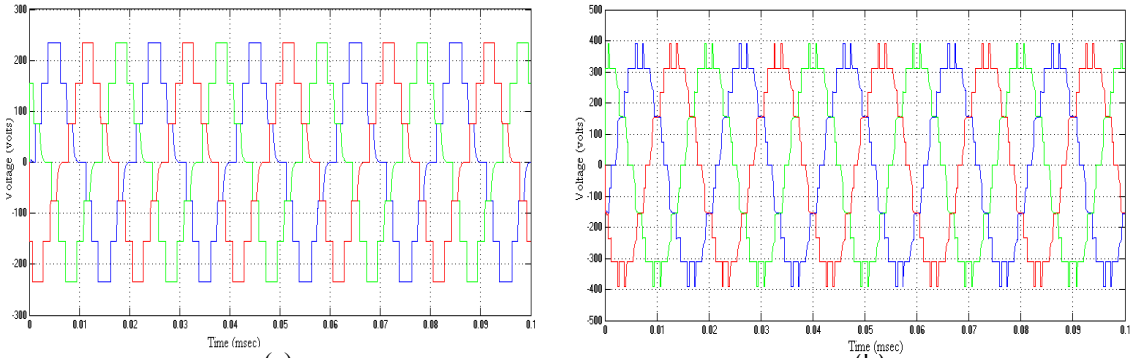
(a)

Figure 6. Switching Pulses for (a) Switches S1, S2, S3, S4, S5 and S6 (b) Switches Q1-Q2 and Q3-Q4



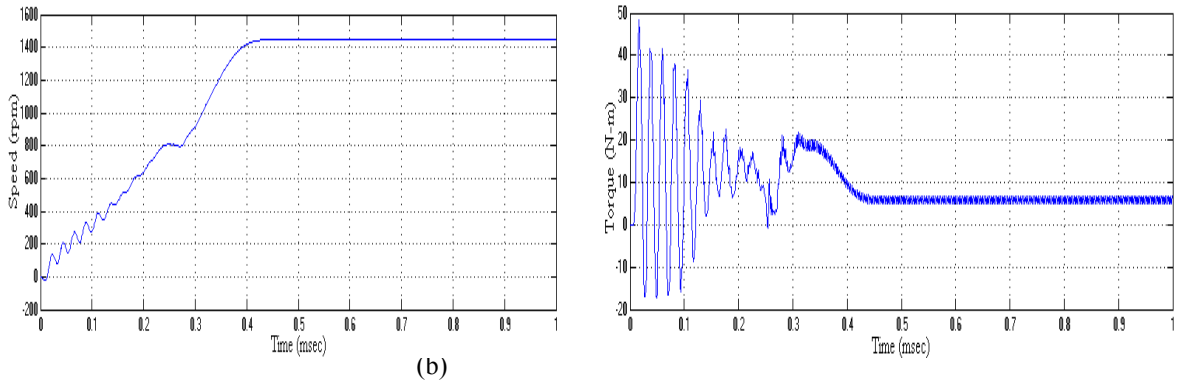
(a) (b)

Figure 7. Output Voltage Waveform for Single Phase (a) Line to Ground (b) Line to Line



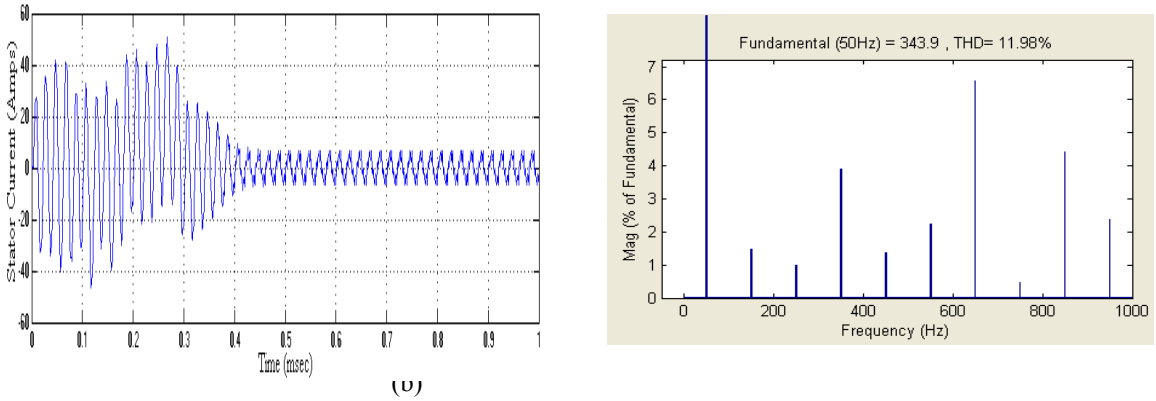
(a) (b)

Figure 8. Output Voltage Waveform for Three Phase (a) Line to Ground (b) Line to Line



(b)

Figure 9. Modified Cascaded Multilevel Inverter fed Induction Motor (a) Speed Curve (b) Torque Curve



(b)

Figure 10. Modified Cascaded Multilevel Inverter fed Induction Motor (a) Stator Current (b) FFT Analysis

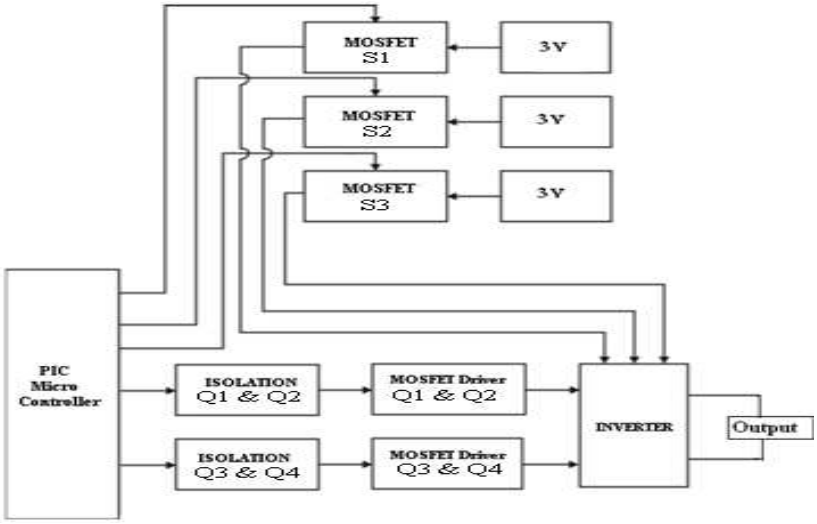


Figure 11. Block Diagram for Modified Cascaded Multilevel Inverter

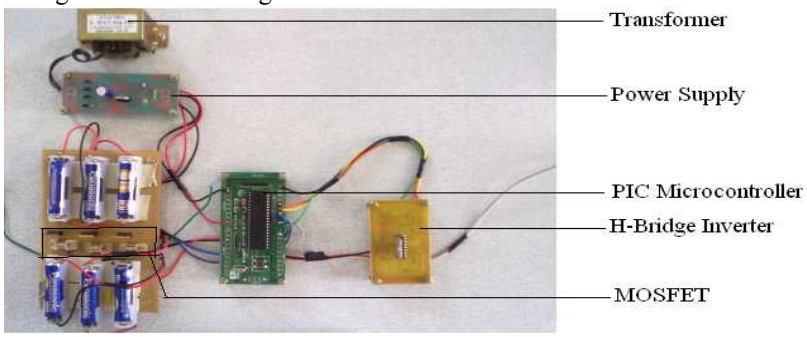


Figure 12. Experimental Setup of Modified Cascaded Multilevel Inverter

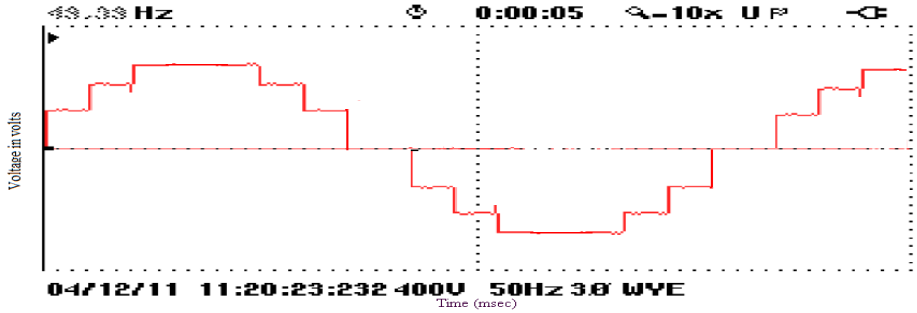


Figure 13. Hardware Output Waveform for Modified Cascaded Multilevel Inverter

Table 1. Basic Operation of Proposed Multilevel Inverter

S. No	Multi-conversion Cell		H-Bridge		Voltage levels
	On switches	Off switches	On switches	Off switches	
1	S1, S2, S3	D1,D2,D3	Q1,Q2	Q3,Q4	$+3V_{dc}$
2	S1, S2, D3	S3, D1,D2	Q1,Q2	Q3,Q4	$+2V_{dc}$
3	S1, D2, D3	S2, S3, D1	Q1,Q2	Q3,Q4	$+1V_{dc}$
4	D1, D2, D3	S1, S2, S3	Q1,Q2	Q3,Q4	0
5	S1, D2, D3	S2, S3, D1	Q3,Q4	Q1,Q2	$-1V_{dc}$
6	S1, S2, D3	S3, D1,D2	Q3,Q4	Q1,Q2	$-2V_{dc}$
7	S1, S2, S3	D1,D2,D3	Q3,Q4	Q1,Q2	$-3V_{dc}$

Table 2. Comparison of Cascaded and Modified Cascaded Multilevel Inverter

Name of Topology	Voltage level on each stage (S)	Number of output level	Number of switches used	Number of switches for 7 level
Cascaded Multilevel Inverter	$1V_{dc}$	2S+1	4S	12
Modified Cascaded Multilevel Inverter	$1V_{dc}$	2S+1	S+4	7

Biography

M.Murugesan was born in Anthiyur on December 27, 1986. He is graduated in 2009 from Anna University, Chennai. He is post graduated M.E Power Electronics and Drives during 2011 from Anna University. He is currently working as Assistant professor at V.S.B Engineering College. His area of interest involves in Power Electronics, inverter, modeling of induction Motor. He is an ISTE life member. He has published more than 10 papers.

S. Sivaranjani was born in Tamilnadu, India, on March 30, 1980. She received B.E degree from Bharathiyar University, in 2001. She also received M.E degree in Power Electronics and drives during 2006 from Anna University, Chennai. She is having 9 years of teaching experience. Currently she is doing Ph.D. Her current research interests include simulation and digital control techniques of AC drives, Inverters topologies and harmonic suppression

G.Asokkumar was born in Erode on June 11, 1980. He is graduated in 2001 from Bharathidhasan University Trichy. He also received M.E degree in Power Electronics and drives during 2011 from Anna University, Chennai. His area of interest involves in Power Electronics, BLDC Drives, inverter, modeling of induction Motor. He has published more than 8 papers

.

R.Sivakumar was born in Madurai on June 4, 1979. He is graduated in 2000 from M.K.University, Madurai and post graduated in 2011 at Anna University of technology, Trichy. . He is currently working as Assistant professor in the department of EEE at VSB engineering College. Karur from April 2006. His research interest involves in power electronics, inverter and modeling of wind turbine. He is an ISTE life member.